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PULSER FOR EMP SIMULATION

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13. ABSTRACT

This development project was undertaken to provide a pulser capable of driving a low-impedance array of antennas with a high-peak-power, short risetime pulse to simulate the electrical interfence effects of an electromagnetic pulse (EMP). The final pulser produced a 100 kilovolt (kV), 72 kiloamperes (kA) output pulse with a 6 nanosecond (ns) voltage risetime and 42 ns current risetime through a single output switch. Additional experiments showed how multiple output switches could reduce the current risetime to 14 ns with a 9 ns jitter. The output switch was a water-or-air-filled spark gap, and operation in both modes is described. The report also includes design information on a simple and reliable 100 kV d.c. switch, a low-impedance high power dummy load, and voltage and current measuring devices for viewing fast transients.

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PULSER FOR EMP SIMULATION

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PULSER FOR EMP SIMULATION

INTRODUCTION

Origin of EMP. The phenomenon of electromagnetic pulse (EMP), first noticed during the Nevada bomb testing, is a high intensity, short risetime transverse electric-magnetic (TEM) wavefront, which radiates spherically from the blast center of a gamma-ray-producing device, such as, a nuclear bomb. The gamma radiation ionizes the air, knocking out electrons, and gives these electrons a velocity vector essentially the same as the incident gamma ray. The moving charges, called Compton electrons, in the earth's static magnetic field are subjected to a radial acceleration into a helical path and radiate their kinetic energy as electromagnetic energy. The intensity and extent of this field depend on the size of the burst, the altitude, and the strength and direction of the earth's magnetic field where the gamma rays strike the atmosphere, but calculations have shown that a single high-yield exoatmospheric burst could cover over half the country with a minimum of 50 kV/meter EMP field.[1] The pulse shape can be represented by a double exponential with a 6 nanosecond (ns) time constant on the leading edge and 300 ns time constant for the trailing edge.

Blast site experiments and simulation studies have shown that EMP can have very serious effects, both transient and permanent, on electrical and electronic equipment.

DISCUSSION

EMP Simulators. To assess the vulnerability of systems and components to EMP effects, several simulators have been built, varying greatly in size, construction, electrical parameters, and field orientation, but all producing approximately the same field strength and pulse shape.[2] Simulators can be generally divided into two classes based on the input impedance of the radiating structure: high impedance - in the order of 100 ohms or higher; and low impedance - in the order of 1 ohm.

High impedance structures are usually preferred where the application allows it because the high voltages and high rate of rise of voltage (dV/dt) are easier to achieve than the high currents and rate of rise of current of the low impedance type. For large fixed-installation facilities, where the equipment is brought to the simulator, the large dimensions required by the high voltages pose no great problem. The larger high-impedance simulators operate at several megavolts (MV).

For transportable facilities, where the simulator is brought to the equipment to be tested, these very high voltages pose great problems, and a lower voltage-higher current system must be considered. The Transportable Electromagnetic Field Simulator (TEFS)[3] is the only available transportable simulator at this time, although others are in the planning stages. TEFS uses an array of dihedral horns to radiate the EM field vertically downward at the equipment under test. The horns are arranged four to a module, series-parallel connected, each module being fed by one 50 ohm RG-14 cable. The modules are all parallel-fed from a common pulser. Figure 1 shows one such module set up in our laboratory; the reel at the top contains 250 feet of cable for connection to the pulser. Figure 2 shows the complete TEFS array of 144 modules, with 25 modules set up over a building.

The van in the foreground contains the pulser and d.c. power supply.

The pulser delivered with TEFS consisted of 12 hand-rolled Mylar-aluminum foil capacitors, connected as shown in Figure 3, discharging through a single output switch. The switch was a mechanically punched, solid-dielectric, two-electrode switch which had to be disassembled and rebuilt after each shot. Operating with half the antenna array, 72 modules, at 60 kV, the risetime was 20 ns and capacitor life was approximately 10 shots before failure. With the full array, the risetime degraded to 25 ns and capacitor life to 2 shots. The operation became tedious, replacing the switch assembly after each shot and the capacitors after every other shot.

Design Goals. At the request of the USA Communications Systems Agency, a program was initiated in this laboratory to substitute an improved pulser for the pulser originally delivered with TEFS. Work on the pulser was begun toward the following design goals for pulsing a quarter array of 36 modules:

Output voltage	100 kV
Load impedance	1.4 ohms, 36 ea. 50 ohm cables
Output current	72 kA
Risetime	6 ns, 10 to 90%
Decay time	300 ns, e- folding

Other desirable features were long capacitor life, no pulse-to-pulse maintenance, and transportability.

Design Theory. If all circuit components were ideal and acted the way that their schematic representations indicate, then a simple RC circuit and switch would produce a zero-risetime, exponential-decay pulse. A 0.21μ F capacitor, charged to 100 kV, switched into a 1.4 Ω load, would produce a 72 kA current pulse with 1/e decay time of 300 ns. The resistances present throughout the circuit are not of major importance, and the stray capacitances are negligible, but the distributed inductance causes great problems. The extremely large values of di/dt ($\approx 10^{13}$ A/s) mean that even minute amounts of inductance cause a large voltage drop (1 nanohenry (nH) $\approx 10^{4}$ volts) and make it difficult to meet risetime requirements. Components which have to withstand the d.c. high voltage for the time it takes to charge the pulser must be more conservatively designed, are large, and as a result have higher inductance. Switches and capacitors which are only voltage-stressed for a few microseconds can have smaller spacings and lower inductance. The two-loop circuit in Figure 4 was used to separate the functions of energy storage and output peaking for the capacitors, and d.c. holdoff and pulse sharpening for the switches. Operation is as follows: Initially, both switches are open and the capacitors are not charged; the primary capacitor is slowly charged from a high voltage, low current supply; and the primary switch, Sp, is closed. The equivalent circuit after switch Sp closes, is shown in Figure 5(a). The current flow, as capacitor C_s is charged, is shown in Figure 5(b), and the voltage across C_s in Figure 5(c).

For the case where C_s is small compared to C_p, the voltage across C_s will resonant charge to $2V_o$, twice the voltage to which C_p is charged, if the secondary switch is not closed. After one quarter cycle of the resonant frequency, C_s is charged to V_o, C_p is still effectively charged to V_o, and a current equal to $V_o\sqrt{C_s/L}$ is flowing in the primary loop. If the secondary switch, S_s, is closed at this time, ignoring for the moment the effect of L_s, the voltage drop across R will be $V_{Cs} = V_c$ and a current equal to V_o/R will flow in the secondary loop. If the primary and secondary currents are equalized by making $C_s = L_p/R^2$, there will be no di/dt in the primary loop and the effect of L_p will be negated. For large values of C_p/C_s, this is the best value for C_s. This equation, and a corresponding one for the case where C_s is no longer negligible compared to C_p, are derived in Appendix C, which includes calculated pulse shapes for switching at times other than one quarter cycle of the primary current.

Figure 6 shows the waveforms at various points in the circuit of Figure 4. The risetime of the load current, I_s, Figure 6(d) depends on the resistance of the load and the inductance, L_s, of the secondary loop. The decay time constant is $R(C_p + C_s)$. This choice of values gives the best overall pulse shape, but the peak voltage across the load is less than the charging voltage. By delaying the firing of S_s to a higher voltage on C_s, or by reducing the value of C_s (underpeaking), the output voltage can be raised at the expense of pulse shape. A dip in the load current occurs after the peak current from C_s. For best pulse shape C_p should be charged to a higher voltage than required across the load. In the final pulser design, the inductance of the primary loop was approximately 110 nH and the load resistance was 1.4 Ω giving a value of C_s for critical peaking of 56 nF; a stack of 8 capacitors in series, 0.5 μF each, giving C_s = 62 nF was used.

EXPERIMENTAL PULSER

a. Distributed Line. The first experimental pulser, shown in Figure 7, consisted of a 0.5 μF - 50 kV - 60 nH tubular energy storage capacitor, C_p, a mechanically closed spark gap switch, S_p, a water-immersed rolled stripline,[4] C_s, a water-filled overvoltaged sharpening gap,[5] S_s, and a copper-sulphate load resistor, R. This and other load resistors are described in Appendix A. The stripline "jellyroll" was pulse-charged from the 0.5 μF capacitor and discharged as a distributed capacitor, or transmission line PFN, through the water-gap. The water-gap assembly was two copper rods, 1¼ inches in diameter and 4 inches long, with their axes parallel, and spacing adjustable up to ½ inch. The first jellyroll was wound from two layers each of 6 by 0.002 inch copper and 18 by 0.005 inch Mylar, 90 feet long, this produced a rectangular output pulse approximately 300 ns long, but punched through before any usable data was obtained. Another line using 8 by 0.010 inch Mylar broke down over the edges of the Mylar. A third line was wound using 3 layers of 18 by 0.005 inch Mylar on each side of the copper, 6 layers in all, and was 10 feet long. Figure 8, (a through e,) shows the voltage pulse across the load resistor, In (a) and (b) the water gap is shorted, disabling the second stage and showing the risetime of the outer loop; in (c) and (d), and (e), the water gap is opened up allowing the jellyroll to be pulse-charged from the first stage before the water-gap connects the second stage to the load resistor. The separate effects of the two stages can be seen best by

comparing (a) and (c); the output of the second stage is over before the first stage has begun to supply the full pulse current.

The cause of the oscillations at the beginning of the pulse was not determined, but it may have been in the measuring circuits rather than from the pulser. It was felt that even though this design produced a fast leading edge it was doomed to poor pulse shape, and the approach was discontinued.

b. Peaking Capacitor. The next design used the same primary storage capacitor, but with the ground return brought up along the sides to form a coaxial geometry for lower inductance. A solenoid was added to the mechanical primary switch for remote firing, the jellyroll was replaced by a lumped peaking capacitor, and the load resistor was a 6 by 6 array of RG-8 cables, each terminated in 50 ohms, first by carbon resistors and later by immersing the cable ends in a salt-water bath. The same water-filled spark gap was used as the secondary switch.

The peaking capacitor was formed between a metal plate, 24 by 32 inches, and the bottom of a 36 inch square metal water tank. Mylar was used as the capacitor dielectric; various thicknesses were used with the best results from 4 layers of 0.005 inch. The Myler layers were put into the tank under water and the bubbles squeegeed out to eliminate air breakdown, which could damage the Mylar. Figure 9 shows the voltage at various sweep speeds across the load at 30 kV, measured with the capacitive divider.

PULSER DESIGN

The data from the two experimental pulsers indicated that a lumped peaking capacitor was a better choice than a distributed capacitor, that adequate risetime could be obtained with a peaking capacitor and water-filled sharpening gap, that the best load for this type of operation was an array of cables terminated in a resistive liquid dielectric, and that the output pulse shape could be controlled by varying the size of the peaking capacitor and the firing voltage of the sharpening gap. One of the problems that appeared was that the acoustic shock in the water gap required that the gap adjusting mechanism be sturdy as well as adjustable in small increments. With these facts in mind, the design was begun on what was expected to be the final pulser. This design phase can be divided into five parts: the primary storage capacitor, the primary d.c. hold-off switch, the peaking capacitor, the sharpening gap, and the cable connections.

a. Primary energy storage capacitor, C_p. The capacitance must be chosen such that the RC time constant, where R is the load resistance, 1.4 Ω, gives the desired pulse decay time. For a decay time constant of 300 ns, C should be 0.21 μF. The capacitor voltage rating has to be at least as high as the charging voltage to be used, approximately 100 kV. The geometry should be coaxial to minimize the inductance of the primary loop. Using capacitors on hand, the primary stack was made up from two Axel 50E102 [illegible] capacitors in series; each one was 0.5 μF, 50 kV, giving the stack 0.25 μF and 100 kV rating. With threaded spacers and bottom plate the stack was 17 inches long and 8$\frac{1}{4}$ inches in diameter. A resistor divider was connected across the two capacitors to ensure that the charging voltage divided

equally between the two capacitors. For very rapid charging (pulse charging) the capacitors alone will divide the voltage equally, and for the static use, or very long charging times, any two equal resistors will give equal division, but for equal division at all times during the charging cycle the RC time constant must be comparable to the charging time. Using 40 megohms total resistance gives an RC of 10 seconds and limits the leakage current at full voltage to 2.5 mA. The sharp edges of the resistor clips at the middle and top of the stack are covered with a metal cylinder and sphere respectively to avoid field enhancement and breakdown problems. The stack with its resistors is shown in Figure 10.

The stack was put into an oil filled cylindrical tank, with cross-section shown in Figure 11, giving the capacitor a coaxial geometry and reducing its inductance. The radial spacing between the capacitor and tank is a compromise between inductance, which decreases with spacing, and voltage hold-off which increases with spacing. The spacing of 2 inches was somewhat marginal, and several arcs occurred between the top of the stack and the tank. With accurate centering, however, the voltage could be raised to 110 kV without breakdown.

One of the enlarged portions of the tank is for the resistor divider network and the other is for a lead to the center of the stack, establishing a half-voltage reference for biasing the center electrode of the three-element triggered switch.

b. Primary switch, Sp. In addition to the manually-and solenoid-actuated atmospheric spark gaps in the experimental pulsers, two pressurized switches were developed for the pulser. The first was a three-electrode, electrically-triggered pressurized spark gap, shown in Figure 12. This switch is similar to a 60 kV switch built at Los Alamos Scientific Laboratory [5,7,8] with the spacings between electrodes increased by a factor of 1.67 for operation at 100 kV. The trigger circuit is shown in Figure 13. The center (trigger) electrode was biased to one-half the operating voltage by connecting it to the midpoint of the capacitor stack. A coupling capacitor in the output of the trigger circuit prevents this bias voltage from shorting to ground through the trigger transformer. This switch worked well up to 85 kV, at 60 PSIG of nitrogen, with reliable triggering and infrequent prefires, but at 90 kV the prefire rate was unacceptable.

Another primary switch was built to raise the voltage hold-off to at least 100 kV. This switch used two electrodes and was fired by opening a solenoid-controlled bleed valve to release the pressure. The electrodes were shaped to a Bruce profile[9] which, like the Rogowski profile, is an approximation of an infinite plane. This gives nearly uniform electric field over the gap and avoids the field enhancement from the edges of the electrode. The profile curve and the generating formula are shown in Figure 14, the cross section in Figure 15, and the assembled switch in Figure 16. The Permally rings reinforce the bakelite cylinder, and the upper metal plate provides field uniformity over the outside surface. At the original spacing of 0.500 inch there was an occasional prefire and a slight loss of pressure control, as seen from the downward curvature of the lower curve of the breakdown voltage plot in Figure 17. The spacing was increased to 0.600 inch and the switch worked well at 110 kV. The lowest voltage at which the switch would fire was 42 kV at sea level and 34 kV at 6000 feet elevation.

c. High Speed Section. This portion of the pulser, consisting of the secondary capacitor, C_s, the secondary switch S_s, and the load connection, was designed as one unit to minimize inductance. Tobe Deutschmann coaxial-disc capacitors were chosen, because of their very low inductance (.1 nH). Because of the 7-8 week manufacturing lead time, units were selected from available stock. One ESC 374 (50 kV, 0.06 μF) and three ESC 361 (20kV, 0.15 μF) were used, giving a capacitor stack of 110 kV, 0.027 μF, 18 inches in diameter, and 3 inches high, with 15 inch diameter annular contact rings top and bottom. This was set on a 22 inch diameter metal ground plane and the water-gap-box placed above it. The secondary switch, or sharpening gap, was two hemispherical-ended 1½ inch diameter stainless steel (304) rods. One was bolted to the metal plate, which was the bottom of the water box; the other was threaded into the center of a 22 inch diameter metal plate above the water box. The load cables came up through the lowest metal plate, with their outer conductors connected to it; the inner conductors were attached to the upper plate with setscrews. The top of the primary switch was connected to the top of the secondary capacitor stack and the bottom of the secondary switch. Figures 18 (a) and (b) show the layout of this pulser.

For a given operating voltage, the spacing of the secondary switch was varied for best output pulse shape. Figure 19 shows the output voltage pulse, measured across the upper and lower plates with the capacitive divider, at 52 kV input charging voltage.

After operating for several hundred pulses, at charging voltages up to 90 kV and variable spacing on the water gap, the secondary capacitor stack failed. The capacitors were returned to the manufacturer for inspection, and it was determined that two of the ESC-361's had shorted. When a charged 0.25 μF capacitor is connected to a discharged 0.027 μF capacitor, the voltage can go as high as 1.8 times the initial voltage, and presumably there were shots where the water gap spacing was great enough to allow the voltage to go high enough to damage the capacitors. Another possible contributing factor was the occasional breakdowns between upper and lower plates along the cable ends, causing voltage reversals on the capacitor stack.

FINAL PULSER DESIGN

Rather than replace the capacitor stack, the pulser was redesigned using the original primary capacitor stack and tank, the two-element pressure-fired switch, and a new high speed section. The changes included raising the voltage rating and capacitance of the secondary capacitor stack, eliminating the cable-end breakdown problem, strengthening the water-gap-box, and eliminating breakdown over the outside surface of the water-gap box. The new capacitor stack was made up of eight Tobe Deutschmann 247-D coaxial disc capacitors, each rated at 0.5 μF, 20 kV, 1nH, giving a stack rating of 160 kV, 0.062 μF. At 100 kV initial voltage on the 0.25 μF capacitor, the maximum voltage on the 0.062 μF stack would be 160 kV, even if the water gap did not fire. The terminal rings of the 247-D were near the center of the disc rather than at the outer edge. This was a disadvantage because the current loop through the capacitors and cable ends is larger, but these were available from the manufacturer's stock with a shorter delivery time.

The water gap box was made from much thicker Lucite, and the lower conductor to it was recessed from the edge to lengthen the surface breakdown path across the box. The lower electrode was changed to a large diameter cone, to reduce inductance, with a copper-tungsten insert to resist erosion. The water gap box and electrodes are shown in Figure 20.

The increased height of the capacitor stack, with the slightly thicker water gap box, resulted in an increase of the exposed cable ends to 13 inches. The upper and lower plates were increased in diameter to 28 inches so that the edge of the plate was 3 inches from the end of the cable. These two changes solved the problem of cable-end breakdown. The pulser, in its final configuration, is shown in Figure 21, and the output voltage pulse, measured between upper and lower plates with the capacitive divider, is shown in Figure 22 for a charging voltage of 80 kV.

CURRENT MEASUREMENTS

Various means had been tried during the development effort to measure the output waveform.[10] No satisfactory current pulse measurement technique was developed and, therefore, measurements were restricted to voltage pulse shapes. After the development of the two-stage version of the pulser was completed, a suggestion of D. Forrester of EG&G, led to a current viewing resistor, which could be inserted in the outer conductor of a coaxial cable. This is described in Appendix B, along with the voltage sensors. Figure 23 is the current pulse in the RG-14 cable to the horn module, viewed at a point 55 feet from the pulser; the 10 to 90% risetime is 42 ns under conditions which are identical to those which produced the 6 ns 10 to 90% voltage risetime in Figure 22.

The difference in measured risetime arises because of inductance in the secondary loop, much of which is in the exposed cable end (360 nH), and because the voltage measurement includes the L di/dt drop across the inductance while the current measurement doesn't. If the pulser generated a step function pulse, the response in Figure 24 would be $\tau = L/R = 360 \times 10^{-9}/50 = 7.2$ ns with 10 to 90% risetime of 16 ns for either one or an array of cables. The inductance of the rest of the secondary loop can be estimated from the observed current risetime of 42 ns. The effect of the inductance common to all cables is multiplied by the number of cables used, in this case 36. Figure 25 shows this circuit; the series inductance is 16.5 nH, exclusive of the cable ends and neglecting mutual inductances.

When the current pulse measurements showed that the risetime was longer than desired, a series of experiments was planned with an array of third-gaps to improve risetime. Before these were begun, the pulser, in the form shown in Figure 21 and operating as shown in Figures 22 and 23, was demonstrated to representatives of SAFCA, MITRE, and EG&G. It was requested by SAFCA that the pulser, with two gaps only, be shipped to Fort Huachuca, Arizona, for immediate use in the EMP testing program. Before shipping the pulser, however, the following tests were made to determine the effects of the third gap and to provide a basis for design of the next generation of pulsers.

THIRD-GAP EXPERIMENTS

The 0.062 μF - 160kV secondary capacitor was replaced by the

ESC-378 0.06 μF-50 kV capacitor and the cable ends were shortened to 3½ inches; the secondary electrodes, in the water gap box, were unchanged. The 10 to 90% risetime was 27 ns with the second gap filled with water and 34 ns with the water removed and the gap operating in air. For air operation it was necessary to increase the spacing by nearly an order of magnitude to optimize the pulse shape.

The cable containing the current sensor was disconnected from the upper plate and four doorknob capacitors, each 500 pF-30kV, were connected in series-parallel between the plates. A small gap was left between the top of the doorknob stack and the cable end for a third spark gap. This circuit is shown in Figure 26, and the current pulse, with a risetime of 17 ns, in Figure 27.

The doorknob stack was replaced with an open-circuited cable, 35 feet long, and the risetime was 14 ns. The 36 load cables were changed to 18 cable pairs with one of each pair connected to the upper plate and open-circuited, the other cable terminated in 50 Ω and with a spark gap to the open cable. Before the gap spacings were optimized the 0.06 μF-50kV capacitor shorted, probably due to overvoltaging.

The 0.062 μF-160kV capacitor stack was reinstalled, and the 18 cable pairs were connected as in Figure 28. The current pulse, Figure 29, has a leading edge risetime of 14 ns, 10 to 90%, but has a half-height step. This step occurs because after the open circuit cable charges and the third gap fires, the charged cable acts like a 50 Ω PFN, discharging into a 50 Ω load, and the voltage divides equally across both.

The third gaps on six of the cable pairs were replaced by spark plugs for more control over the gap spacing, Figure 30, and the jitter between firing times of these third gaps was measured. The voltage pulse on the load side of the third gap, for each of six different cable pairs, was used as an external trigger to view the current pulse in the one load cable which contained the viewing resistor. The jitter between the earliest and latest of the six pulses was approximately 9ns.

If time had permitted, one or more of these third-gap schemes would have been included in the delivered pulser and would have improved the risetime considerably. Figure 31 shows six traces of load current, using the output voltage from each of the six spark plugs in turn for the trigger signal. The risetime has been degraded by extra cables between the sensor and the scope for delay time matching.

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE DESIGNS

A comparison of the risetime results of the multiple output gaps (third gap experiments) with the single output gap, shows that the extremely high values of di/dt required through the single output gap are unattainable, and that by dividing the output current among a number of gaps, which corresponds to raising the load impedance on each gap, risetimes can be significantly improved. These results, also, show that the slight improvement shown when the second gap is water-filled, as opposed to air-filled, is not worth the difficulty of water-sealing and acoustic shocks.

The effect of inductance in the stripped-back ends of the output cables where they attach to the pulser is serious, and lengthening this end to avoid flashover is a bad compromise. A better approach would be encapsulation or immersion in oil or water.

The design for a future pulser should include a lower-inductance d.c. storage capacitor to ease the burden on the second and third stages, gas-pressurized second and third gaps, disc capacitors with large diameter contact rings for the second stage, and open-circuted cables, for the third-stage capacitors. Two or more unequal length open-circuited cables could be used for each load cable, and their lengths could be varied for pulse shaping.

The array of third-gaps should be in a circle around the second gap, physically placed so that the ultraviolet light from the second gap would prime all the third gaps; the gas enclosure should be outside the third gaps rather than between the second and third gaps. This UV priming would reduce the jitter, or statistical firing time variation, between the various output gaps. Another approach to jitter control would be to prime the gaps with a UV laser shortly before firing the pulser.

To reduce inductance, the current path from the load side of the second gap to the third gaps should be through a conducting ring rather than individual cable ends.

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APPENDIX A

Load Resistors

Three different types of load resistors were used during the development project - bulk liquid, cables with carbon resistors, and cables with liquid electrolytes. The first bulk liquid resistor was made with a Lucite housing, a saturated copper sulphate-deionized water solution, and copper plates 6" wide, 8" high, and separation variable from zero up to 4 inches. The resistance was varied by adjusting the spacing to minimize voltage oscillatons and to try to achieve critical damping. There was a considerable amount of unnecessary inductance in this load. Another liquid electrolyte resistor was made, with a spacing, determined from the first model, of approximately 1 inch. Both of these resistors were used in the water tank holding the jellyrolland the water-filled spark gap. Neither was completely satisfactory; besides being difficult to connect, the inductance was too high and the resistance was difficult to control and measure, because of electrolysis effects.

The second approach to the load resistor problem was with multiple coaxial cables, each terminated with one or more resistors. At the feed end, the cables were joined into a 6 by 6 array as in Figure A-1 and connected to the pulser with 6 X 0.002 inch copper straps. The termination impedance at the load ends of the cables was investigated with time-domain-reflectometry. When carbon resistors were used, the cable end was stripped back just enough to connect the resistor between the center conductor and the braided outer conductor; all carbon resistors were 1 watt rating. A single 50 ohm resistor had a voltage reflection coefficient ρ of 0.42 and inductance of 13.4 nanohenries. With two resistors, 22 and 27 ohms, in series, ρ was 0.47 and L was 27.2 nH. Two 100 ohm in parallel gave ρ = 0.30 and L = 7.5 nH; three 150 ohm gave ρ = 0.26 and L = 6.5 nH. The inductances occur at the transition from coaxial to lumped resistor geometry and are determined from the TDR trace. One of the cables was terminated with an "Ohm-Weave" card, a woven nichrome resistor, but this was quite inductive, with 1600 nH.

The carbon resistors were satisfactory from the standpoint of matching, but were unable to withstand repeated pulses at high voltage. The three parallel 150 ohm resistors exploded around 20 kV and the series pair around 27 kV.

The most satisfactory approach found to date for a low impedance, high peak power load is the array of coaxial cables terminated in an electrolyte. A solution of sodium chloride in deionized water was used, and the configuration of the cable end and the salt concentration were varied for optimum results. Figure A-2a shows the configuration for the best match and was obtained with a saturated solution, which is desirable for ease and repeatability. Figure A-2b is a time-domain-reflectometer trace of this cable end; the inductance is 0.42 nH and capacitance is 4.8 picofarads (pF). At higher voltages, typically 35 kV, sparking occurred in the salt solution around the end of the outer conductor because of high current density. To overcome this problem, the shape shown in Figure A-3a was adopted, reducing current density by spreading the current over the surface of the ball.

The inductance is due to the uncancelled magnetomotive force in the stripped-back cable end and increases with the length of the stripped-end. The capacitance is due to the displacement current in the water (dielectric constant = 78) between the ball and the braid, and decreases with increasing stripped length. The dimensions shown are a reasonable compromise with inductance of 6.4 nH and capacitance of 9.6 pF, calculated from the TDR trace in Figure A-3b. The concentration of salt is adjusted for a match to 50 ohms after the inductive and capacitive components have died out. The cables used were RG8A/U and were 40 feet long; this gave a free time of approximately 100 ns before any reflection from the load arrived at the pulser.

This load was used up to 100 kV with no problems in the salt water load itself. After several thousand pulses, between 40 and 100 kV, the cables deteriorated in voltage holdoff strength and began failing at pulse voltages as low as 60 to 65 kV.

APPENDIX B

Measuring The Output Pulse

The first measurement attempts used high-input-impedance scopes and commercial voltage dividers, e.g., the Tektronix 1000X, 50 kV probe and the Pacific Power Designs 2000X, 350 kV capacitive divider. The strong radiated fields from the pulser, along with the large area and unshielded nature of the dividers, made the noise problem severe and almost totally obscured the pulse observation.

A low-impedance, very fast sweep speed scope, the Tektronix 519, was used next, but low impedance dividers had to be developed to use with it. One divider that was tried with the bulk liquid load was a 50 ohm coaxial cable (RG 58) stripped back so that the center conductor was exposed to the electric field in the liquid. This type of load was abandoned in favor of the cable loads before any decision was reached on the usefulness of this measurement technique.

Most of the measurements during the pulser development were made with a capacitive divider designed to work with the low impedance of the 519 scope. Referring to Figure B-1, the voltage attenuation factor is $(C_1 + C_2)/C_1$ or approximately C_2/C_1, where $C_2 >> C_1$. To avoid pulse "droop" due to capacitor charging, the time constant of the lower part of the divider had to be large with respect to the expected pulse lengths to be measured. Choosing $RC_2 = 50C_2 = 1.5 \times 10^{-6}$ (five times the 1/e decay time of the pulse) requires that C_2 be at least 30 nF. Using 1 mil Mylar film as the dielectric, an area of 45 square inches was needed. Nearly all the applied voltage must be held off across C_1 so 6 layers of 10 mil Mylar were used there; for an attenuation factor of 1000, the area of C_1 was made 2.7 square inches. The divider structure is shown in Figure B-2.

Another feature of this divider is that if C_1 breaks down, as happened a few times, the scope is protected from the full pulser voltage of 100 kV by the puncturing of the 1 mil Mylar. Figure B-3 shows the voltage trace during a failure of C_1 at 25 kV. The scope and attenuator, with 600 volt ratings, were not damaged.

Two current viewing resistors were made to view the current in the outer conductor of one of the load cables. A 1 ohm resistor was made from 10 paralled 10 ohm carbon resistors, Figure B-4, and the output from this was cut in half by the two 100 ohm resistors in series. A lower inductance resistor; Figure B-5 was made with eleven nichrome strips replacing the outer conductor of the load cable; the resistance was approximately 0.1 ohm. The inductance of this resistor is 0.4 nH as computed from the TDR trace, Figure B-6.

APPENDIX C

Theory of Peaking Capacitor

The actual two-loop circuit with a sharpening gap and peaking capacitor is shown in Figure C-1a. Two assumptions can be made to simplify the analysis: (1) the inductance in the secondary loop affects only the leading edge of the pulse rather than the overall pulse shape, and (2) with Cp >> Cs, the voltage on Cp does not change significantly during the charging of Cs and Cp can be replaced by a constant voltage source. These assumptions will be dropped in the more detailed analysis. With these assumptions, the circuit becomes as shown in Figure C-1b. For the time prior to t_o, the closing of the secondary switch,

$$Ip(S) = \frac{Vo/Lp}{S^2 + \frac{1}{LpCs}} ,$$

$$ip(t) = Vo\sqrt{\frac{Cs}{Lp}} \sin \frac{t}{\sqrt{LpCs}} ,$$

$$V_{C_s}(S) = \frac{Vo/LpCs}{S(S^2 + \frac{1}{LpCs})} , \text{ and}$$

$$V_{C_s}(t) = Vo\left(1 - \cos \frac{t}{\sqrt{LpCs}}\right) .$$

At $t = \frac{\pi}{2}\sqrt{LpCs}$, the optimum time for closing the second switch, $i_p(t) = Vo\sqrt{\frac{Cs}{Lp}}$ and $Cs(t) = Vo$. Letting these be the initial conditions and changing the time bases so that t = o when the second switch is closed

$$\begin{bmatrix} LpS + \frac{1}{CsS} & -\frac{1}{CsS} \\ \frac{1}{CsS} & \frac{1}{CsS} + R \end{bmatrix} \cdot \begin{bmatrix} Ip(S) \\ Is(S) \end{bmatrix} = \begin{bmatrix} L\, ip(o) \\ V_{C_s}(0)/S \end{bmatrix} = \begin{bmatrix} Vo\sqrt{\frac{Cs}{Lp}} \\ Vo \end{bmatrix}$$

and $$Is(S) = \frac{Vo}{RS}\left[\frac{S^2 + \frac{1}{\sqrt{L_pC_s}}S + \frac{1}{L_pC_s}}{S^2 + \frac{1}{RC_s}S + \frac{1}{L_pC_s}}\right]$$

Letting $\sqrt{L_pC_s} = RC_s$ makes $Is(S) = \frac{Vo}{RS}$ and $i_s(t) = \frac{Vo}{R}u(t)$, a step function of amplitude Vo/R starting when the second switch is closed.

This is the optimum condition wherein the effect of the inductance L_p has been completely negated by the peaking capacitor C_s and the second switch. The waveforms for this circuit are shown in Figure C-2. In designing a pulse modulator, the load resistor, R, is fixed by the application and L_p is the unavoidable distributed inductance of the energy storage capacitor or capacitor bank. The peaking capacitor, C_s, is chosen by satisfying $\sqrt{L_p C_s} = RC_s$, or $C_s = L_p / R^2$. For the pulser described in the text $R = 1.4\ \Omega$ and $L_p = 110$ nH, calculated from the ringing frequency of the primary loop. For these values, $C_s = 56$ nF. Figure C-3, shows the results of computer calculations (using ECAP) of the load voltage pulse shape $V_R(t)$, with $R = 1.4\ \Omega$, $L_p = 110$ nH. and C_s as a parameter. The pulse shape for the optimum value of C_s (i.e. 56 nF) is a step function, while for values less than this (underpeaking) there is droop following the leading edge. For larger values of C_s (overpeaking) the total risetime (from zero to peak load voltage) is deteriorated. For all values of C_s the curves approach unity for the steady state solution. Figure C-4 shows the total risetime for varying C_s. With the above assumptions, the risetime is zero for $C_s < L_p / R^2$ and increases sharply for larger values of C_s.

For practical circuits, the assumption that C_p is so much larger than C_s that C approximates a constant voltage source is not valid. In the actual circuit, $C_p = 250$ nF, $C_s = 56$ nF, and the voltage on C_p is down to 82 percent of the initial charging voltage when the current in the primary loop is a maximum. The circuit in Figure C-5a shows the actual circuit before the closing of the switch in the second loop, where Vo is the initial charging voltage on C_p.

$$I_1(S) = \frac{Vo/Lp}{S^2 + \frac{1}{L\,Ct}},$$

$$V_{C_s}(S) = \frac{Vo}{LpCs}\left[\frac{1}{S\left(S^2 + \frac{1}{LpCt}\right)}\right],$$

$$i_1(t) = Vo\sqrt{\frac{Ct}{Lp}}\,\sin\frac{t}{\sqrt{LpCt}}, \text{ and}$$

$$V_{C_s}(t) = Vo\,\frac{Ct}{Cs}\left[1 - \cos\frac{t}{LpCt}\right],$$

where

$$Ct = \left[\frac{1}{Cp} + \frac{1}{Cs}\right]^{-1} = \frac{Cp\ Cs}{Cp + Cs} .$$

At $t = \pi \sqrt{LpCt}\ /2$,

when i_1 (t) is a maximum, i_1 (t) = Vo $\frac{Ct}{Lp}$

and V_{C_s} (t) = Vo $\frac{Ct}{Cs}$ = V_{C_p} (t). Using these values as the new initial voltages and current, and changing the time base so that t = o corresponds to the closing of the switch in the second loop, the circuit in Figure C-5b exists, where

$$\begin{bmatrix} \frac{1}{SCp} + \frac{1}{SCs} + LpS & -\frac{1}{SCs} \\ \frac{1}{SCs} & \frac{1}{SCs} + R \end{bmatrix} \cdot \begin{bmatrix} I_1(S) \\ I_2(S) \end{bmatrix} = \begin{bmatrix} LVo\sqrt{\frac{Ct}{Lp}} \\ \frac{Vo\ Ct}{SCs} \end{bmatrix} .$$

and $$I_2(S) = \frac{Vo\ Ct\ Lp\left[S^2 + \frac{1}{\sqrt{CtL}}S + \frac{1}{CtL}\right]}{LRCs\ S^3 + Lp\ S^2 + \frac{RCs}{Ct}S + \frac{1}{Cp}} .$$

When the second loop switch closes, i_2 (t) rises instantaneously to V_{C_s}/R = VoCt /CsR, and at this time i_1 (t) = Vo $\sqrt{Ct/L}$.

Equating these currents to minimize Lp $\frac{di_1(t)}{dt}$ and the effect of Lp gives Lp = $\frac{Cs^2R^2}{Ct}$

and

$$I_2(S) = \frac{VoCt}{RCs}\cdot\frac{\left[S^2 + \frac{1}{RCs}S + \frac{1}{R^2Cs^2}\right]}{\left[S^3 + \frac{1}{RCs}S^2 + \frac{1}{R^2Cs^2}S + \frac{Ct}{Cs^3R^3Cp}\right]} .$$

Note the symmetry between the numerator and denominator of this expression. The optimum value for Cs is found from the positive root of Lp = $\frac{Cs^2R^2}{Ct}$,

$$Cs = -\frac{Cp}{2} + \sqrt{\left(\frac{Cp}{2}\right)^2 - \frac{LpCp}{R^2}} \quad .$$

The actual circuit had an estimated 10 nH of inductance in the second loop. Figure C-6 shows the load voltage pulse shape for the circuit of Figure C-5b with the addition of the 10 nH inductance and Cs as the parameter. Figure C-7 shows the dependence of total risetime (zero-to-peak) on Cs. The risteime for Cs = 56 nF (from the constant-voltage-source analysis) is 26 percent higher than for the Cs = 47 nF best-pulse-shape criterion. Figure C-8 shows the risetime for 10-90 percent of peak load voltage. The curves also show that if a drooping or oscillating waveform can be tolerated (i.e., the lower curves in Figure C-6) the risetime can be reduced further.

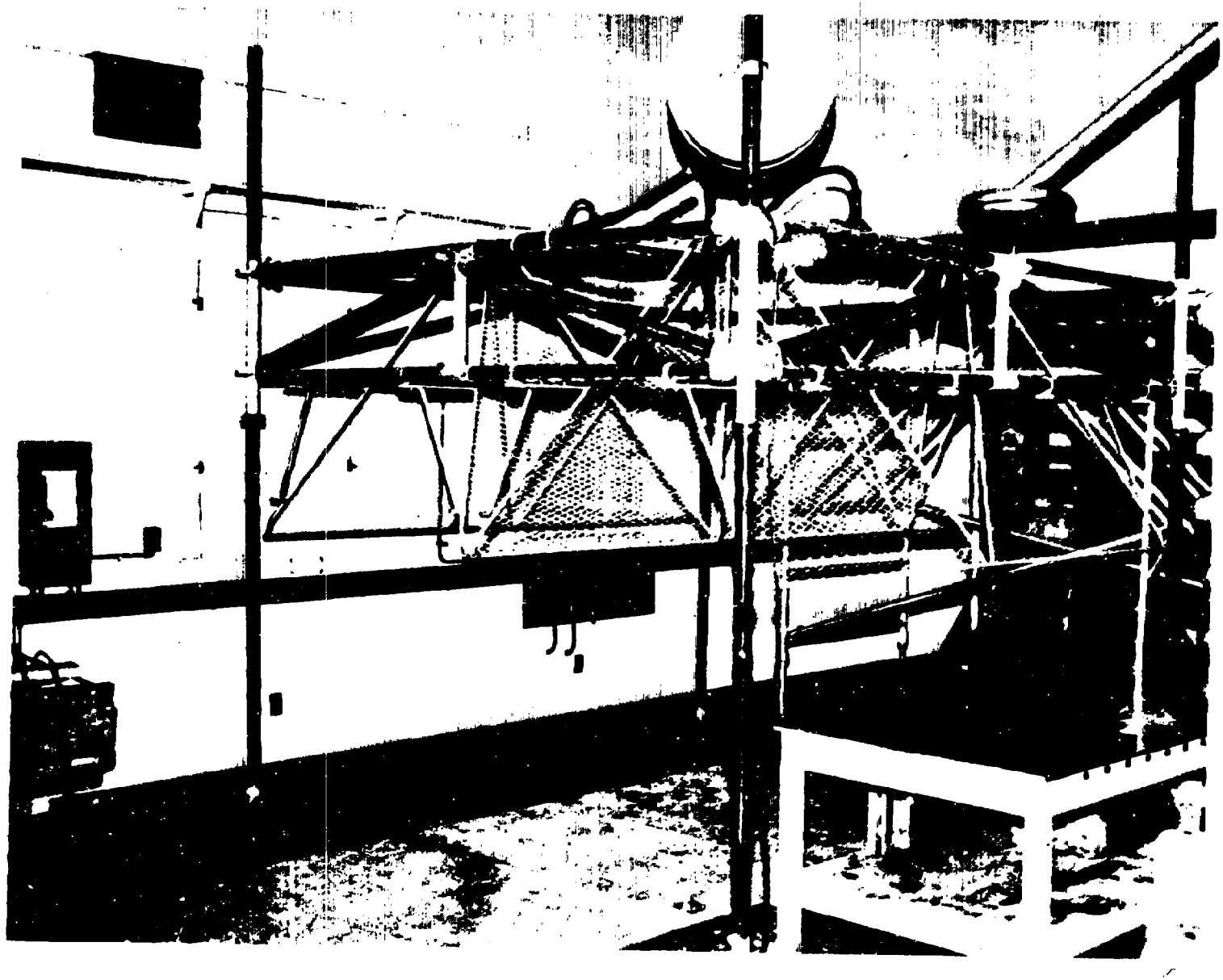


Figure 1. Radiating Horn Module

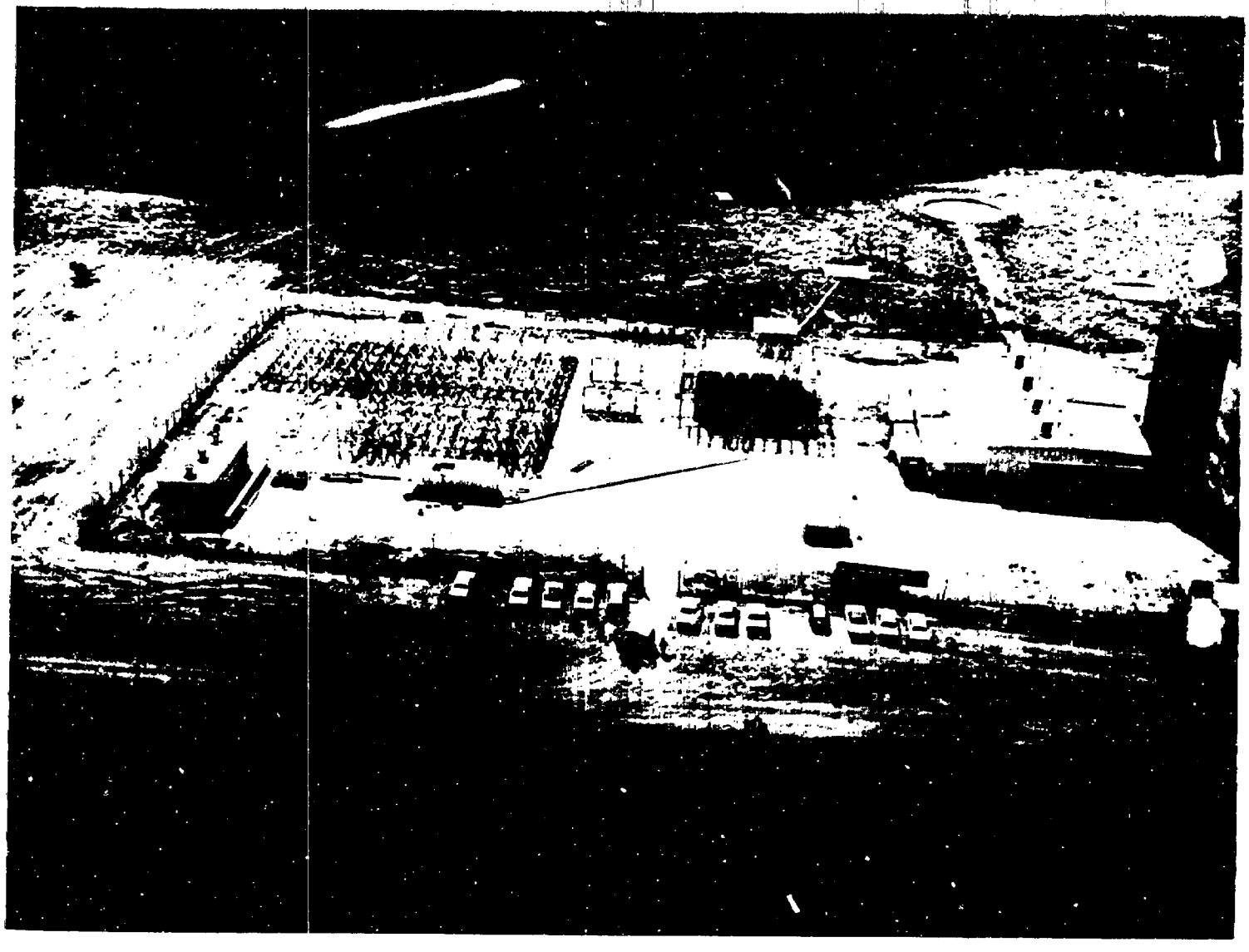


Figure 2. TEFS Array at west Range, Fort Huachuca, Ariz.

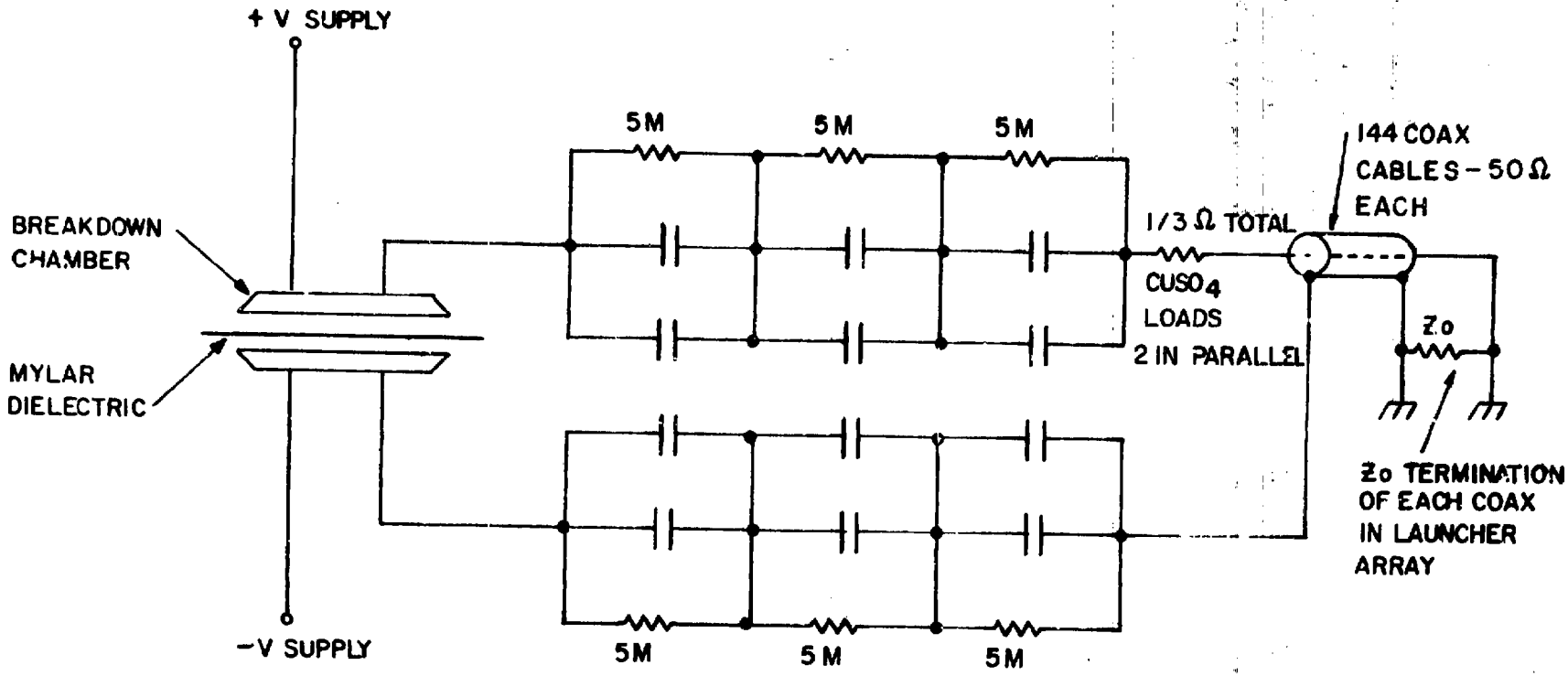


Figure 3. Electrical Equivalent of the Pulser

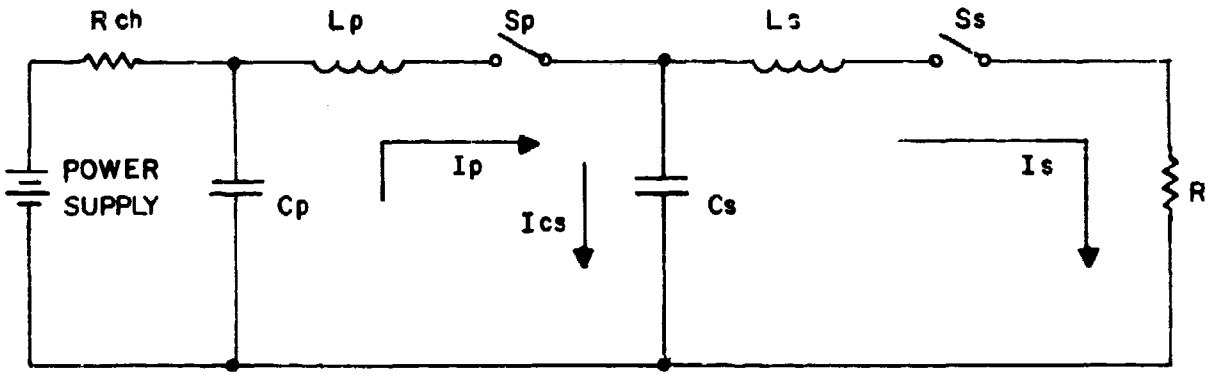


Figure 4. Two-Gap Pulser Circuit

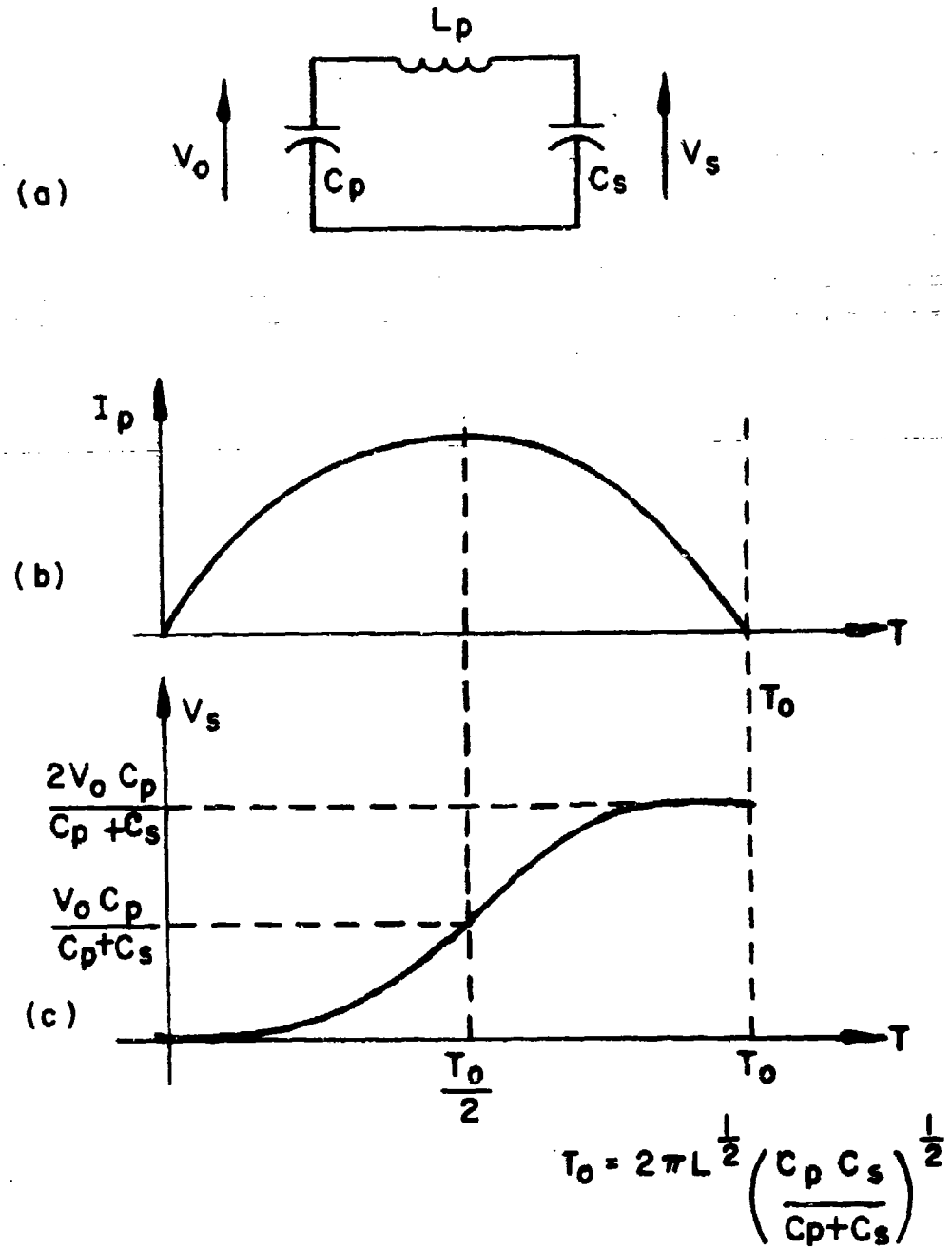


Figure 5. Waveforms During Charge Transfer

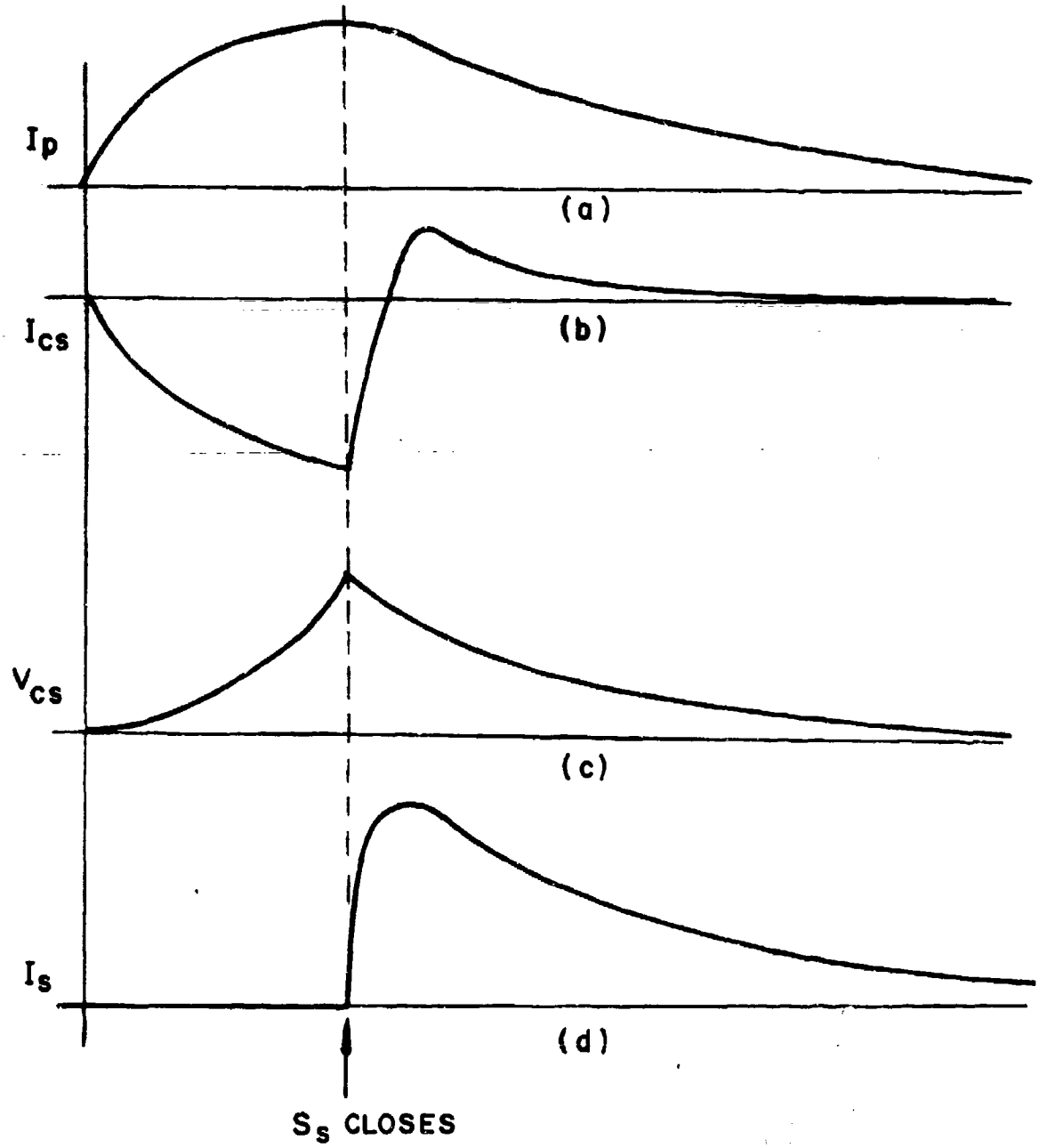


Figure 6. Waveforms in Two-Gap Pulser

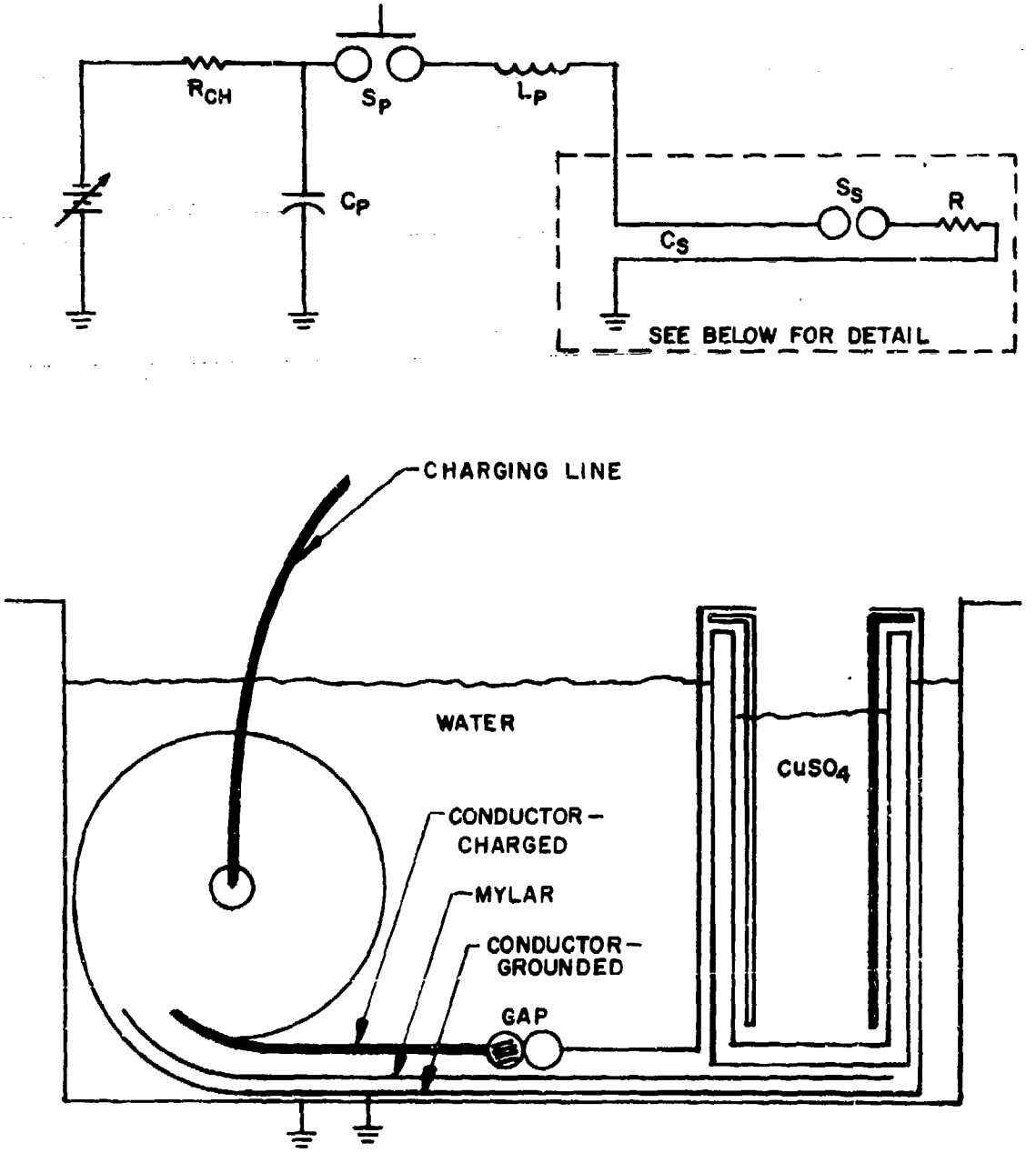


Figure 7. Distributed Line Pulser

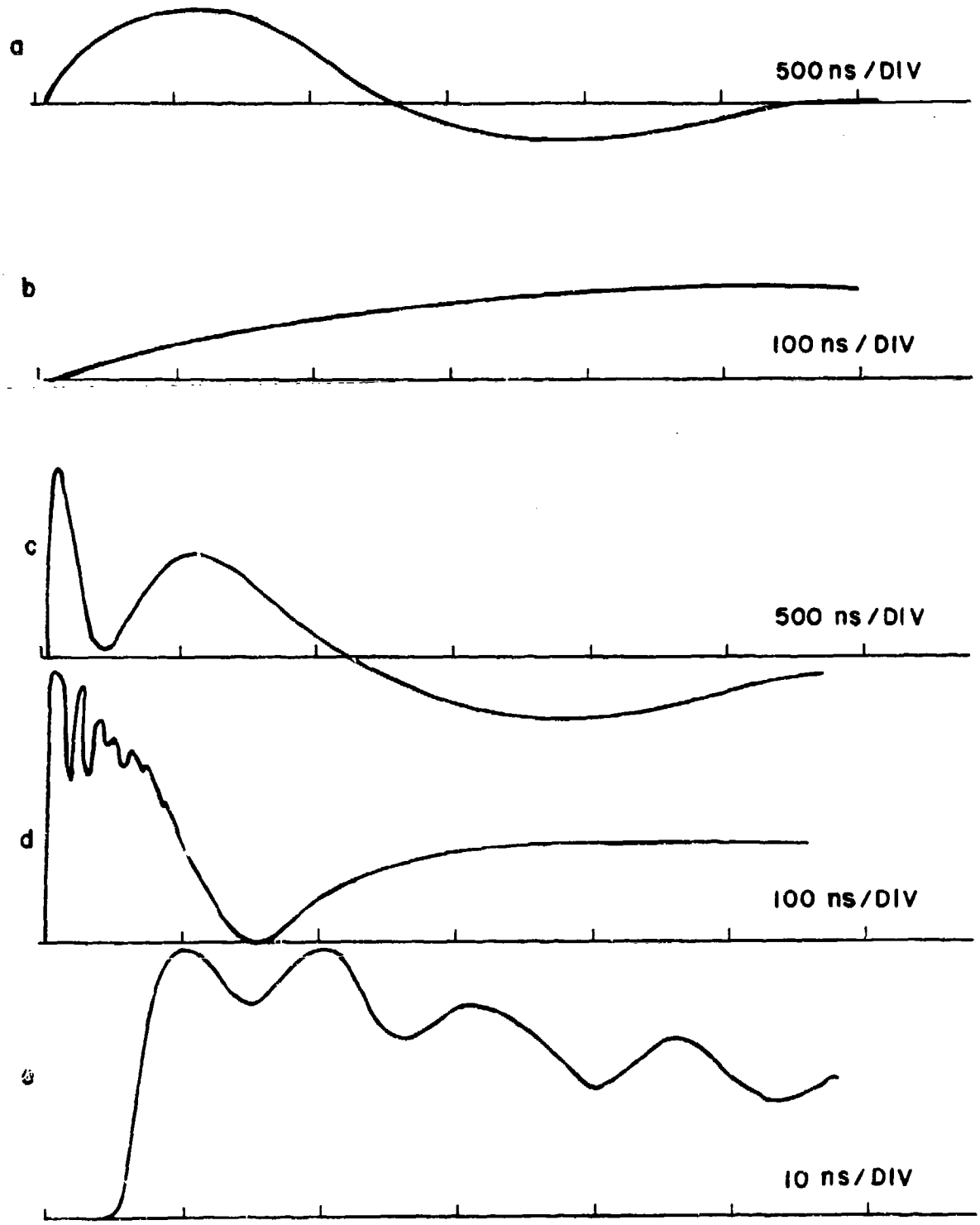
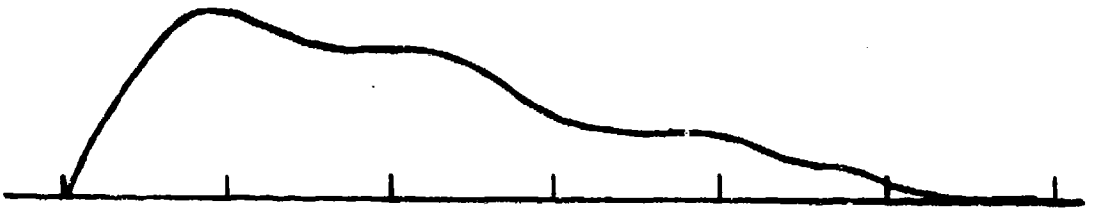
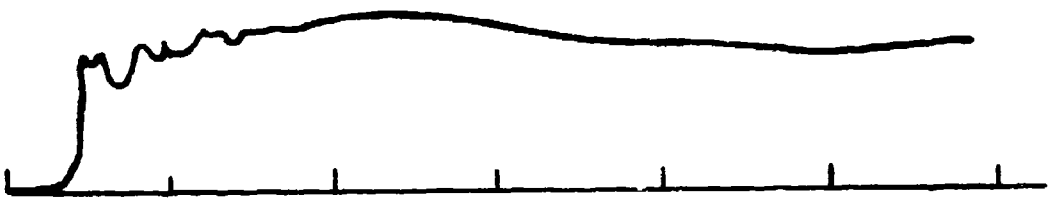


Figure 8. Load Voltage

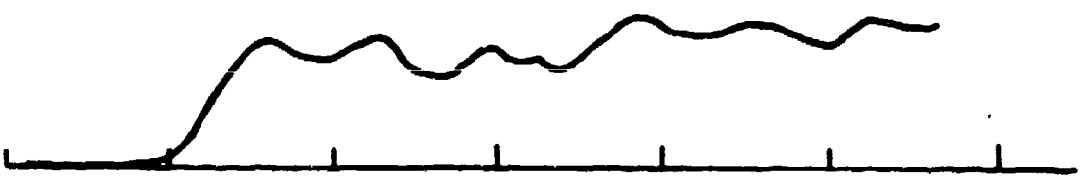


(a) NO SHARPENING GAP, 200 ns/DIV

(b) 0.005" GAP, 200 ns/DIV



(c) 0.005" GAP, 50 ns/DIV



(d) 0.005" GAP, 10 ns/DIV

Figure 9. Output Voltage Pulse

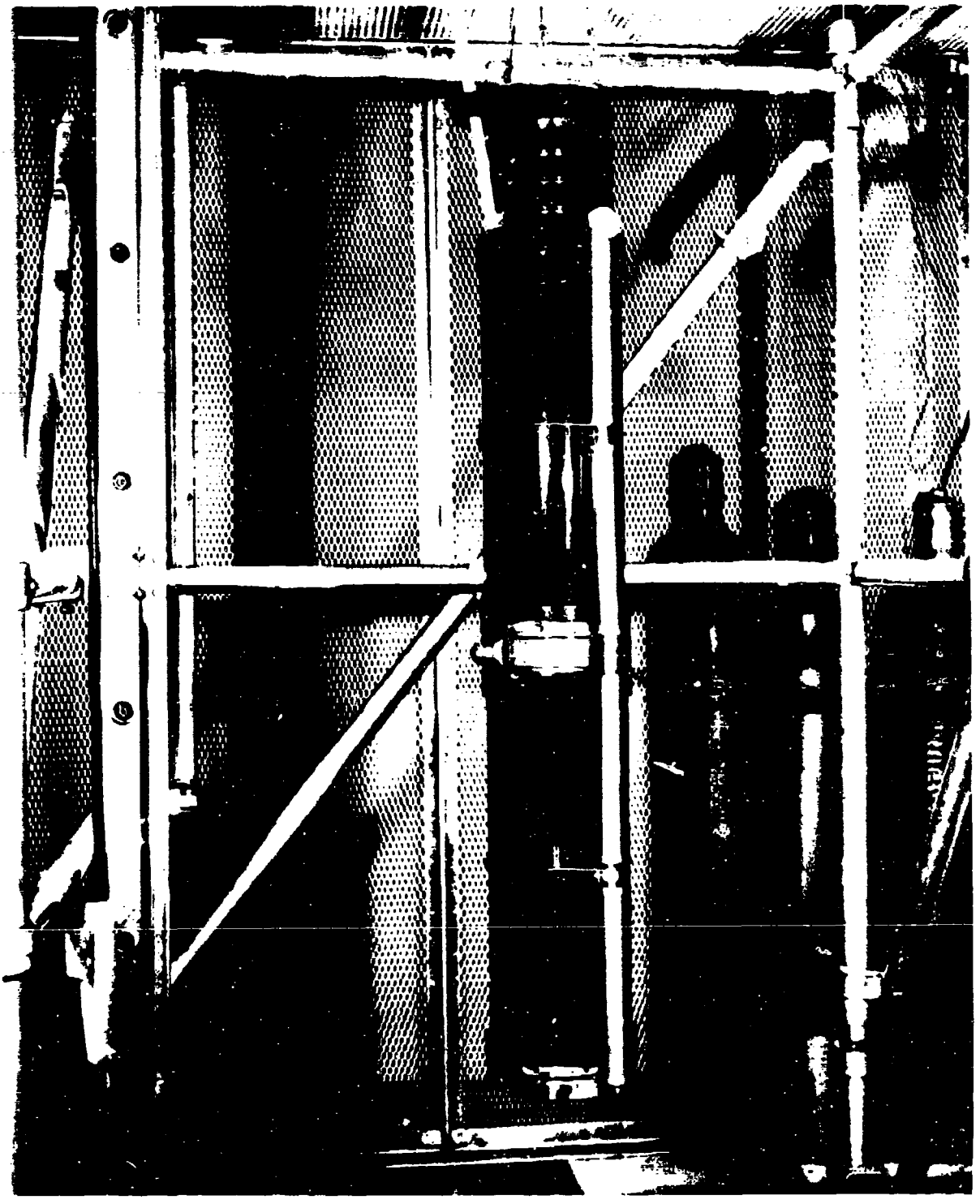


Figure 10. Primary Capacitor Stack with Primary Switch

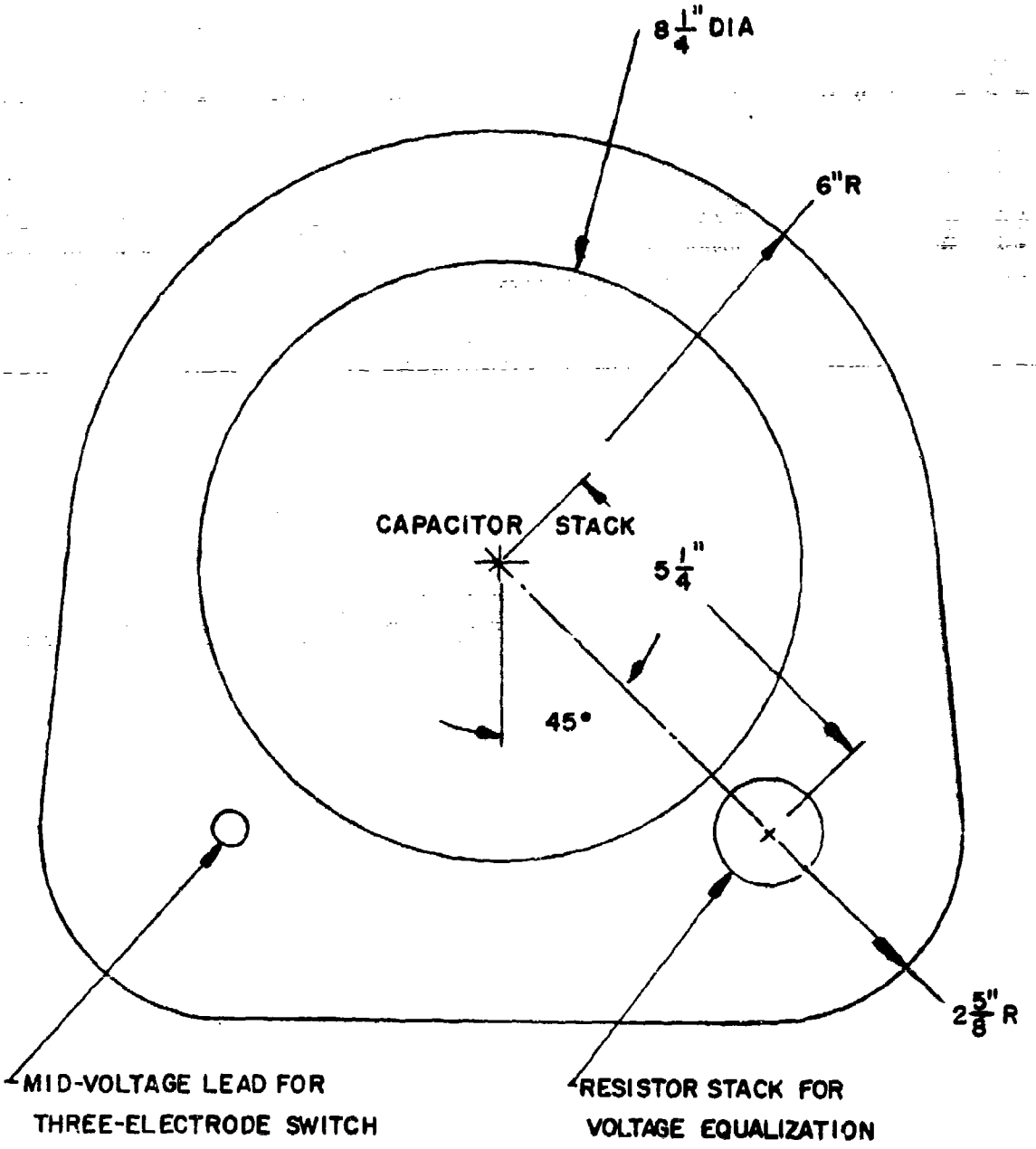


Figure 11. Cross Section of Capacitor Oil Tank

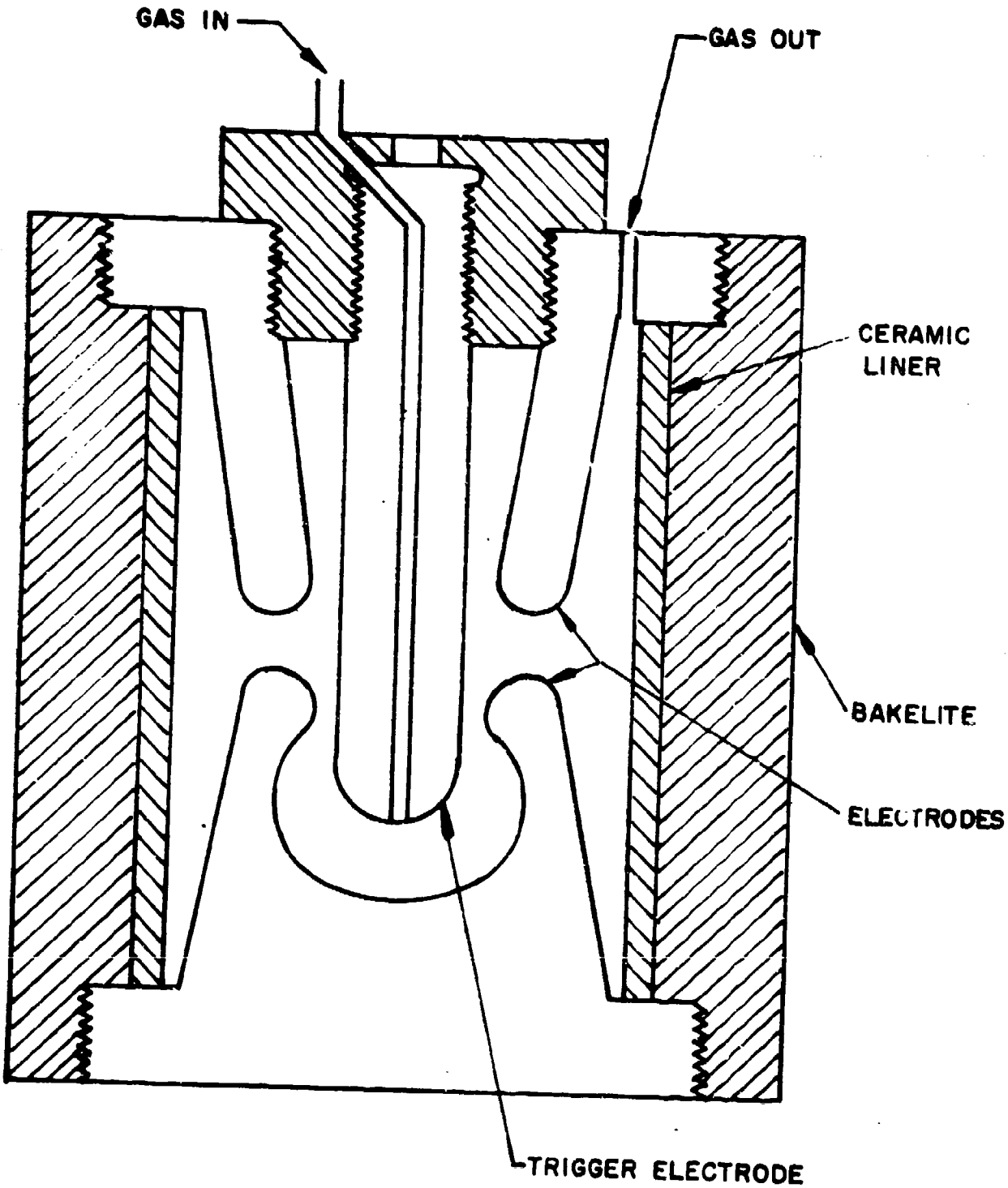


Figure 12. Triggered Spark Gap

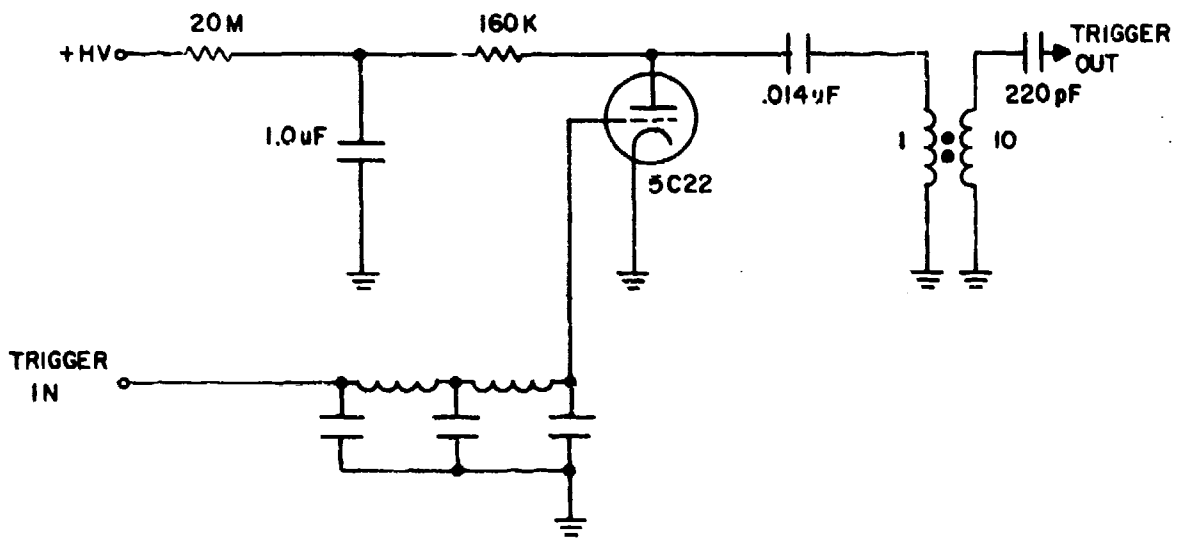
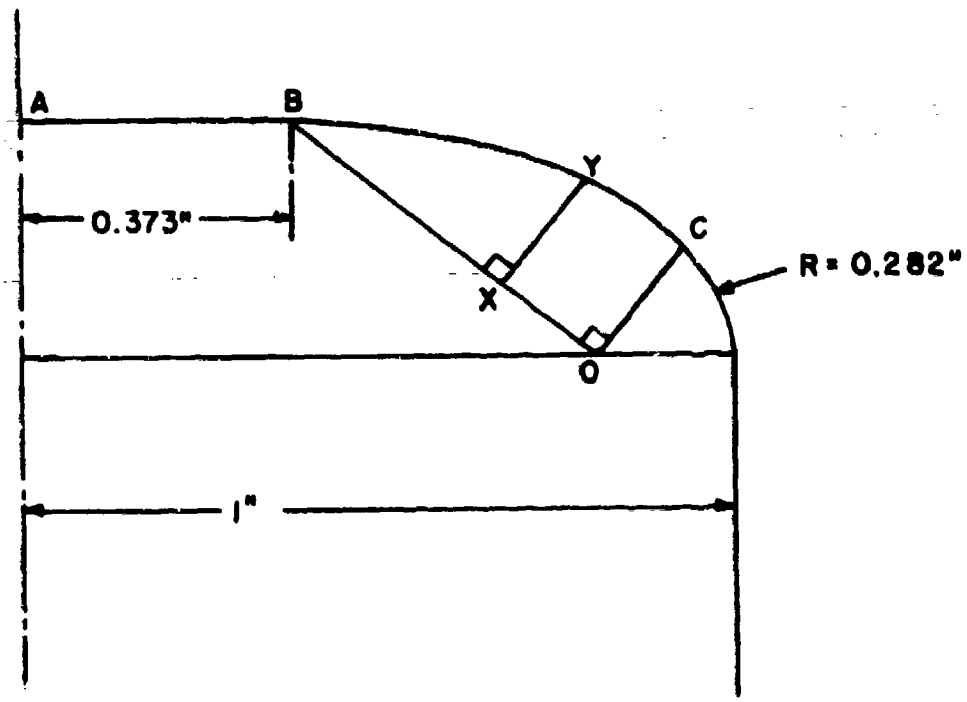


Figure 13. Trigger Circuit



$$XY = CO \sin\left(\frac{BX}{BO} \cdot \frac{\pi}{2}\right) = 0.282 \sin\left(\frac{BX}{0.502} \cdot \frac{\pi}{2}\right)$$

Figure 14. Bruce Profile for 2" Diameter Electrode

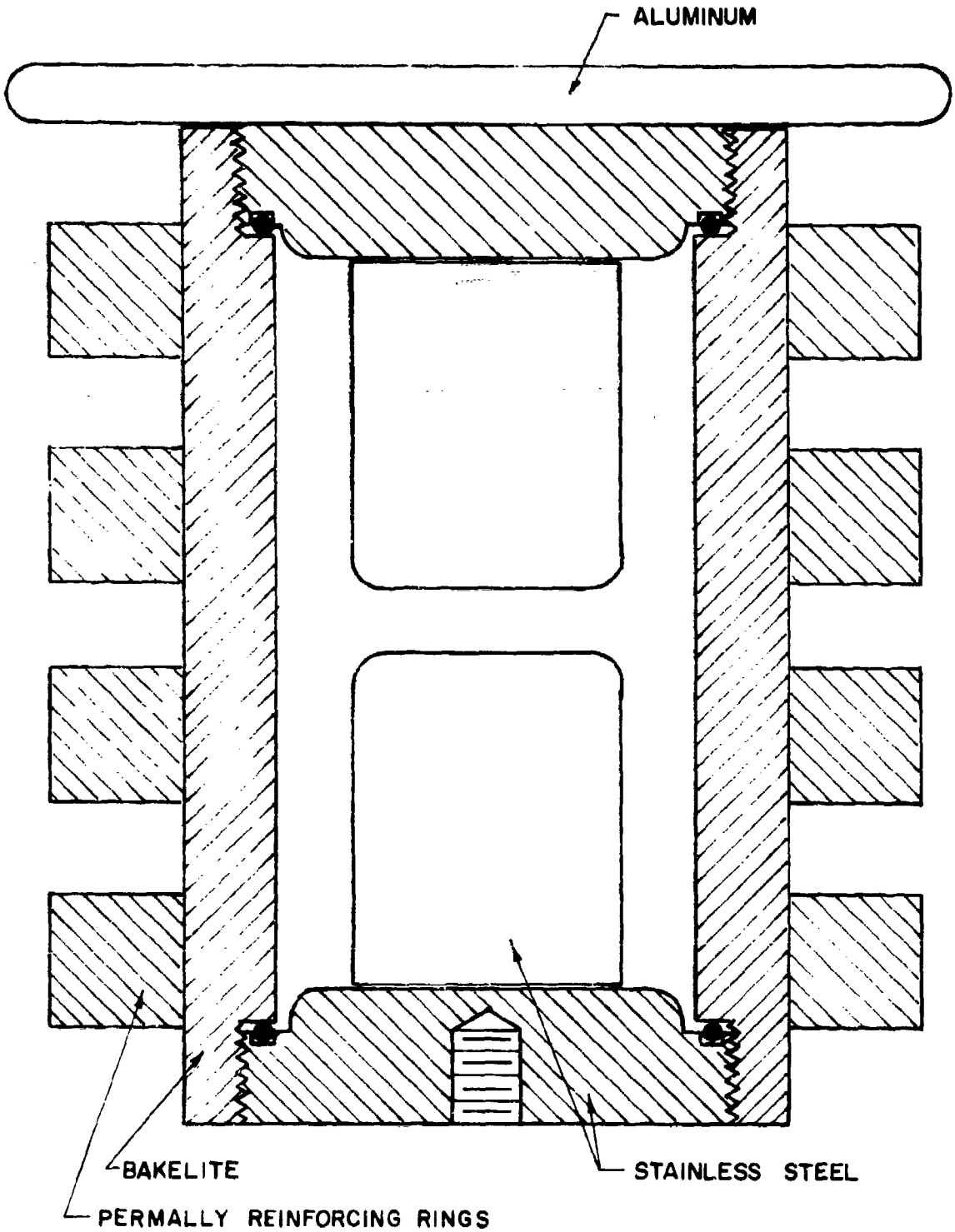


Figure 15. Two-Element Pressure-Fired Switch with Reinforcing Rings

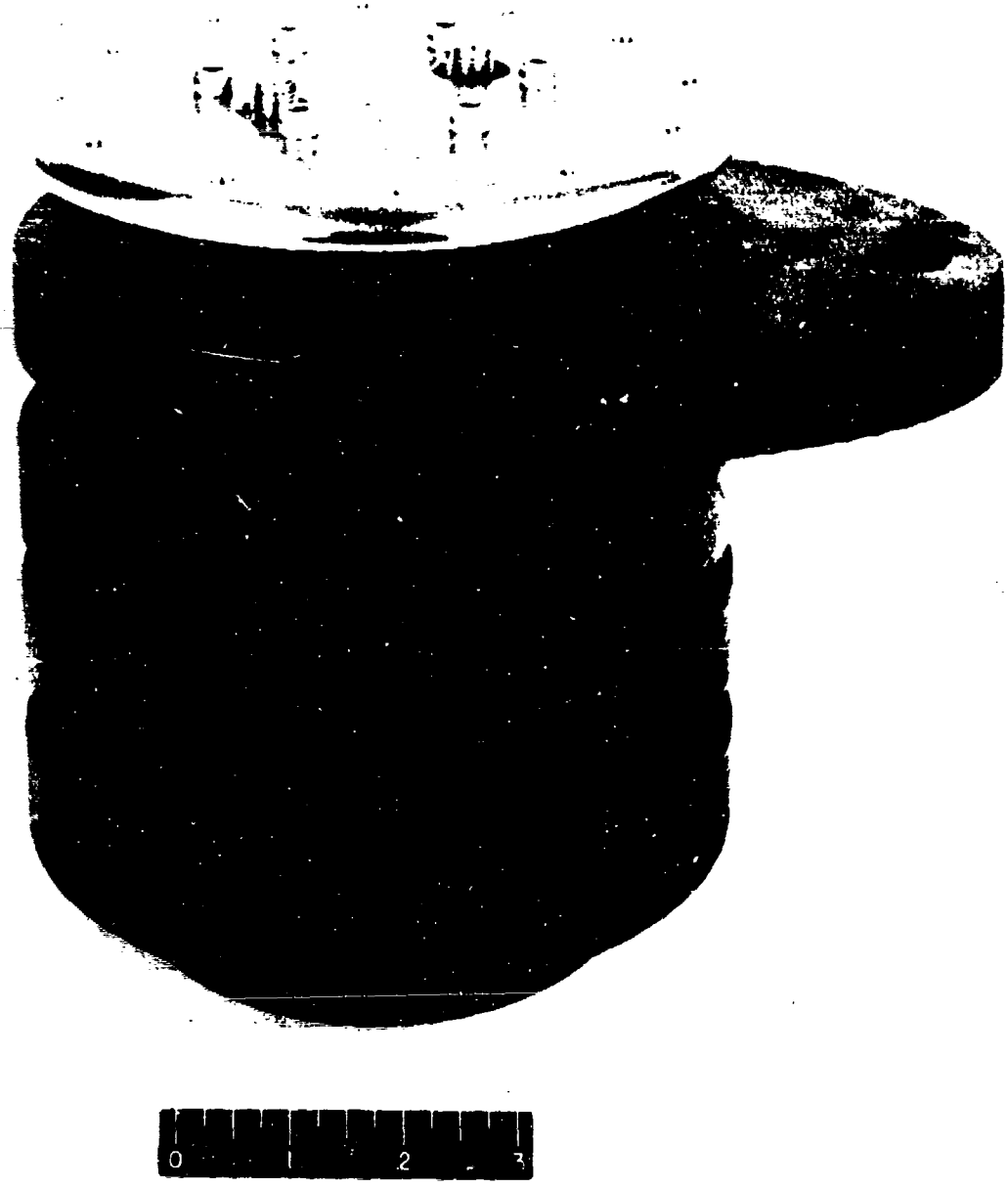


Figure 16. Primary Switch for EMP Pulser

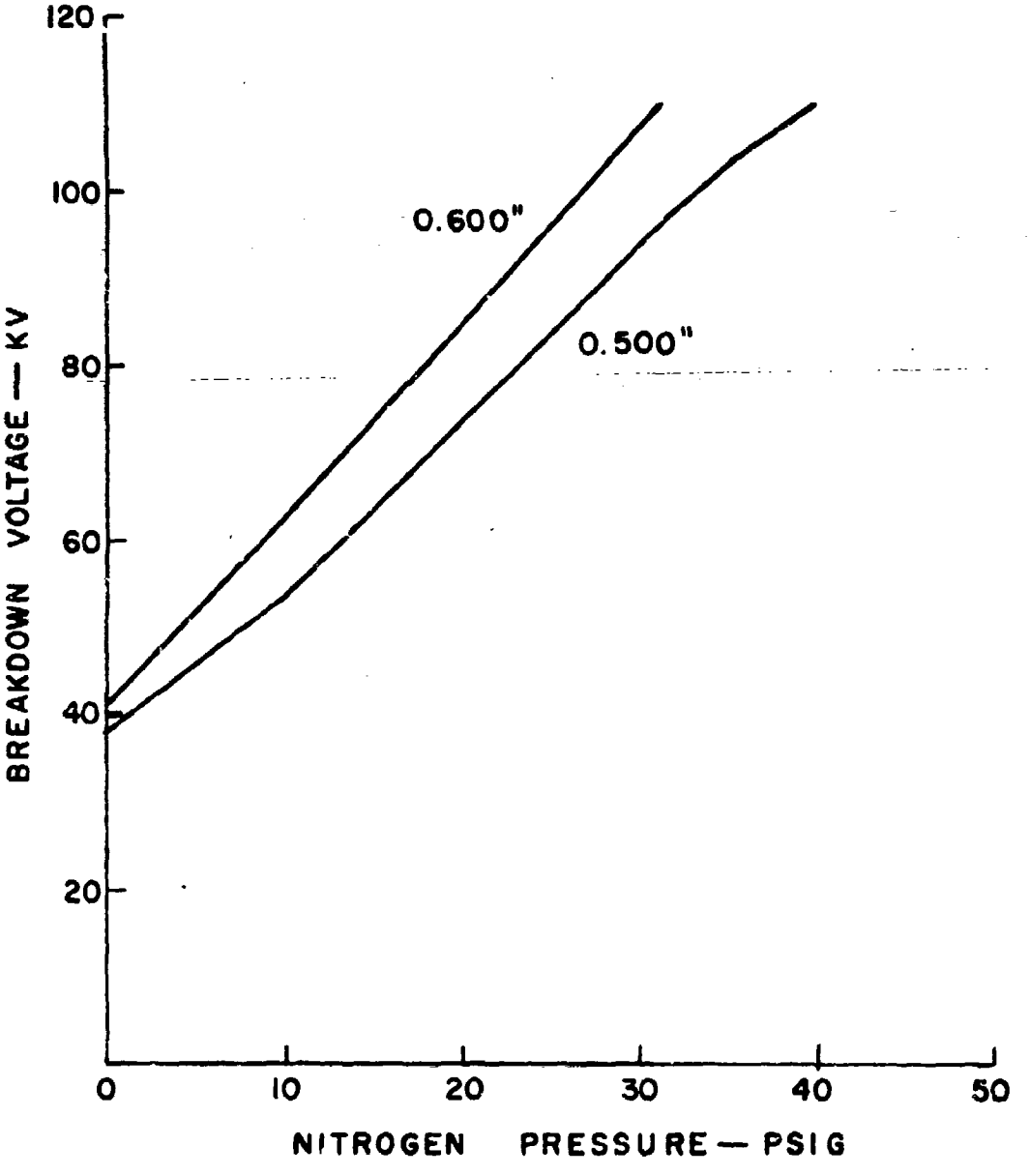


Figure 17. Breakdown Voltage Versus Pressure for Bruce Profile Switch

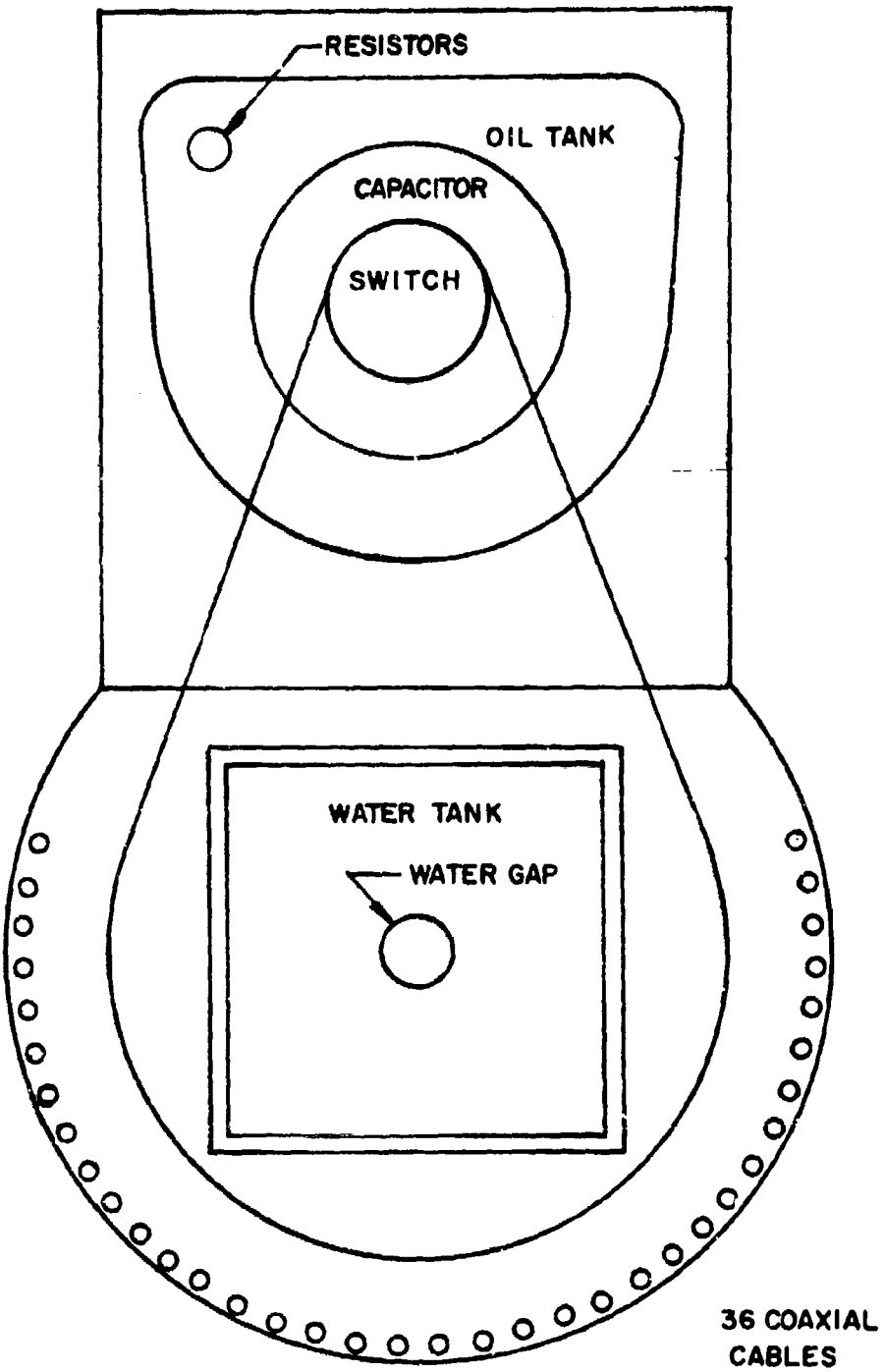


Figure 18(a). Pulser, Top View

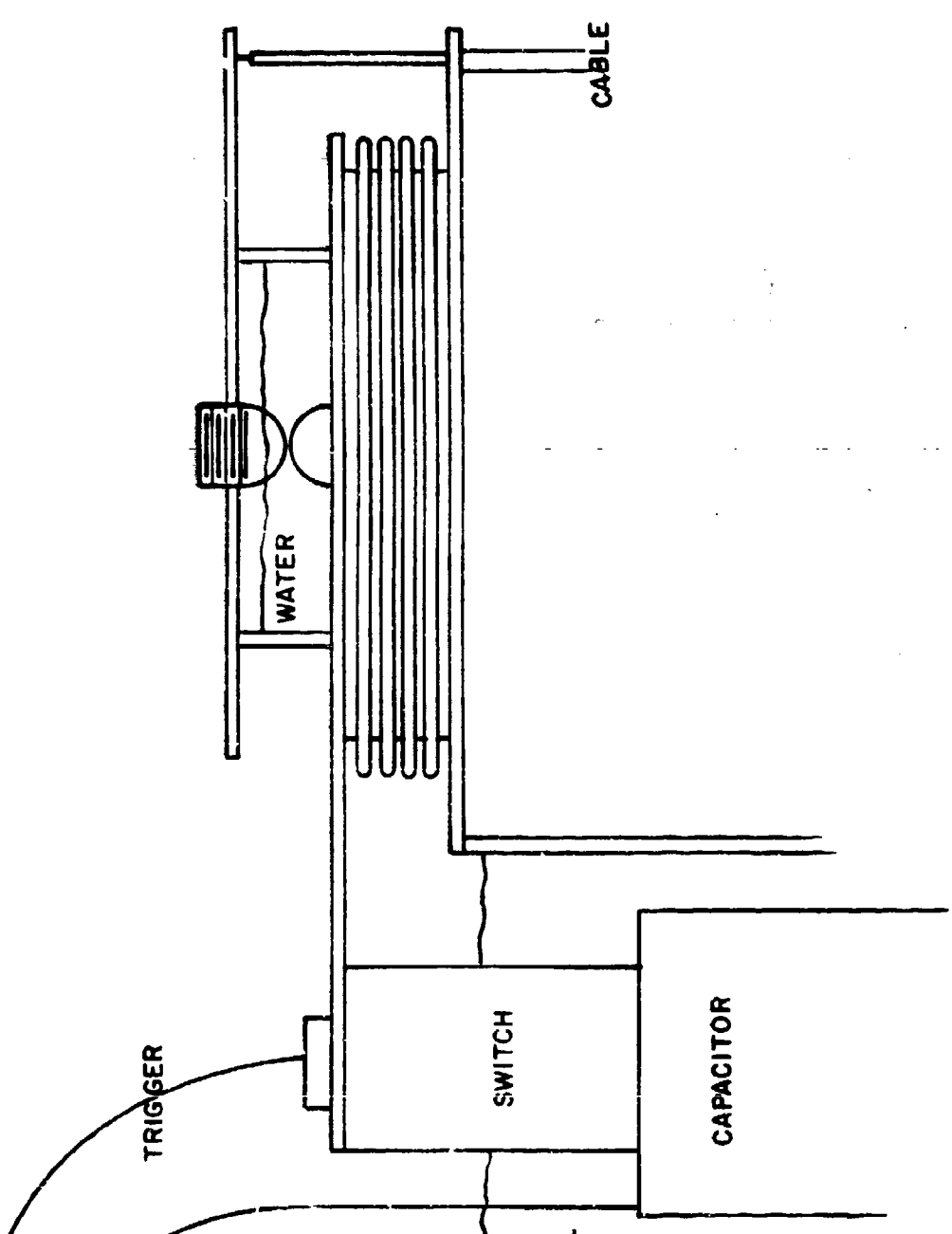
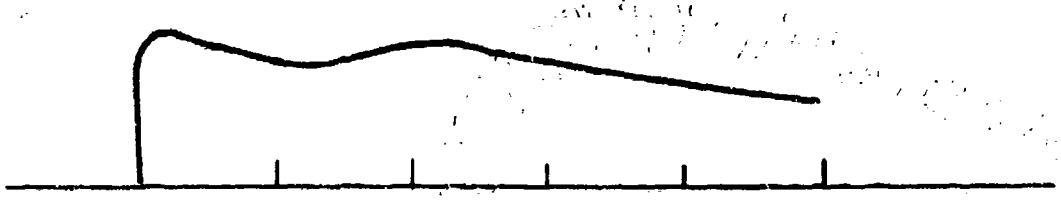
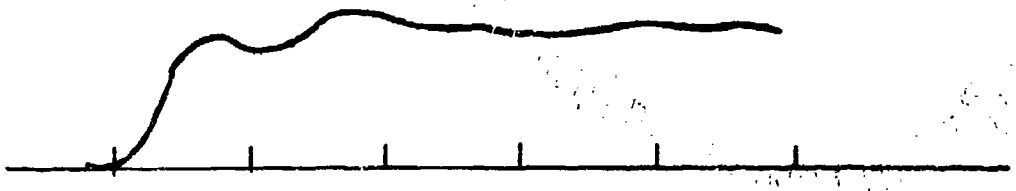


Figure 18(b). Pulser, Side View

(a) 200 ns / DIV



(b) 100 ns / DIV



(c) 20 ns / DIV

(d) 10 ns / DIV

Figure 19. Voltage Output at 52kV Charging Voltage

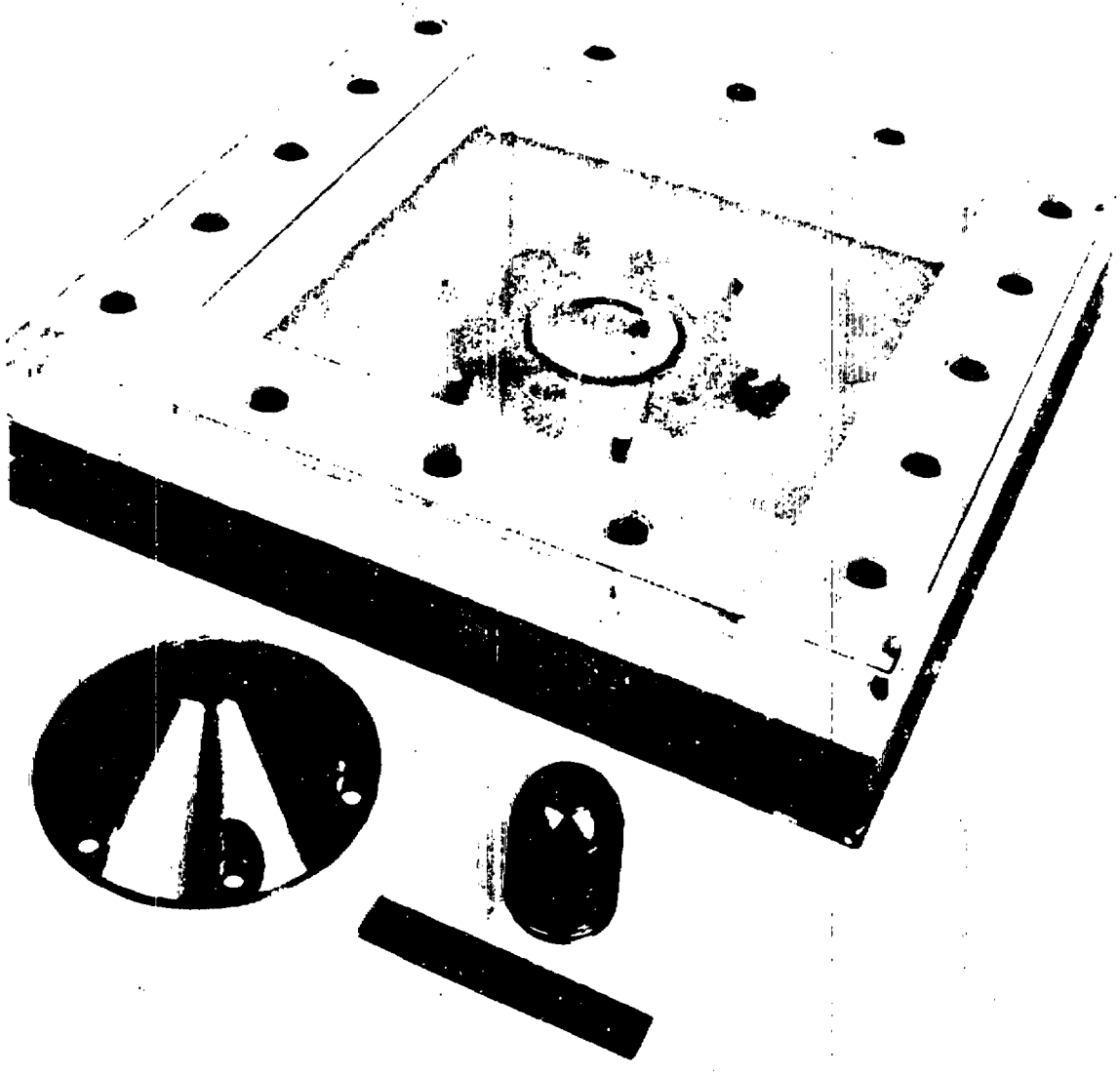


Figure 20. Water-Gap Box and Electrodes

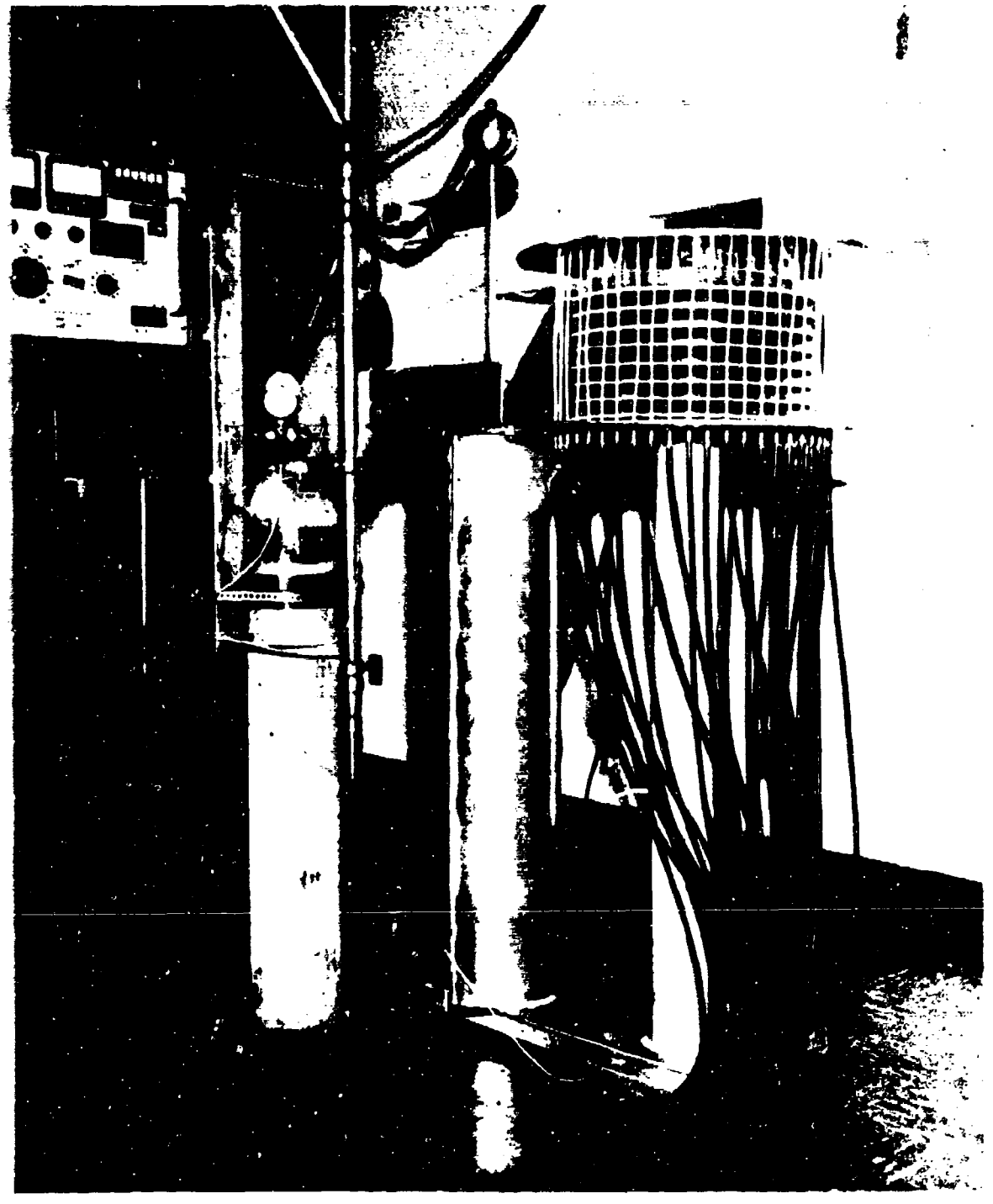


Figure 21. Final Two-Gap Pulser

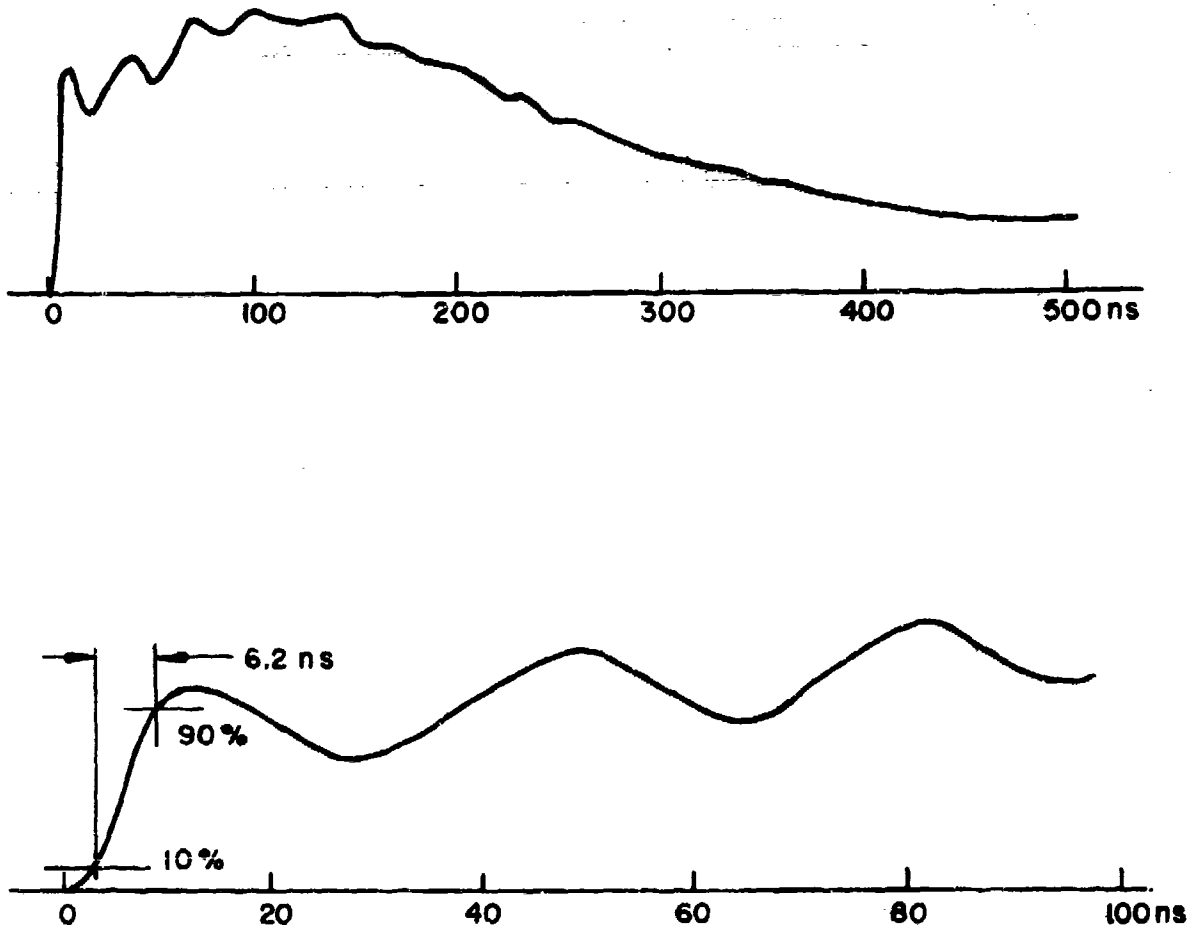


Figure 22. Output Voltage Pulse

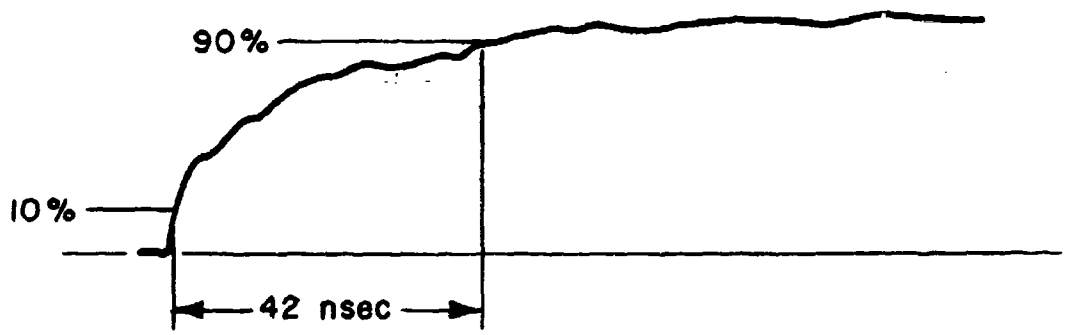
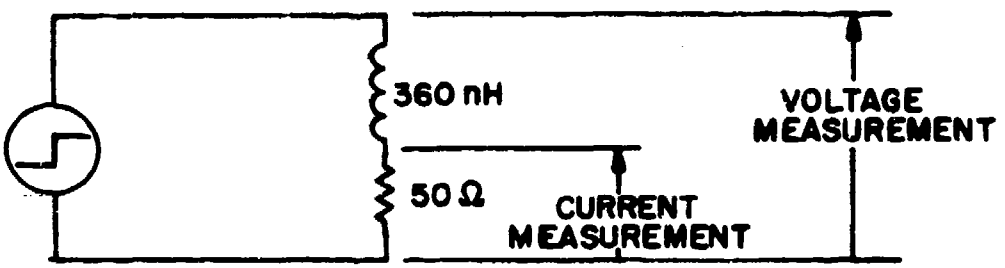
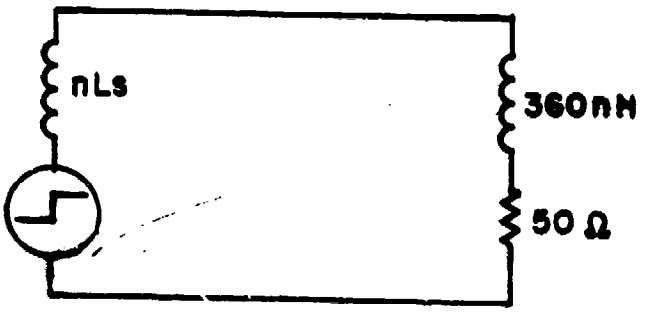


Figure 23. Current Pulse in RG-14 Cable



$$\tau = \frac{L}{R} = \frac{360 \times 10^{-9}}{50} = 7.2 \text{ ns}$$

Figure 24. Step Pulse into L-R Load



$$\tau = \frac{nLs + 360 \times 10^{-9}}{50} \quad , \; Ls = 16.5\,nH$$

$\tau = 19.1$ nsec FOR $n = 36$

Figure 25. Step Pulse with Series Inductance

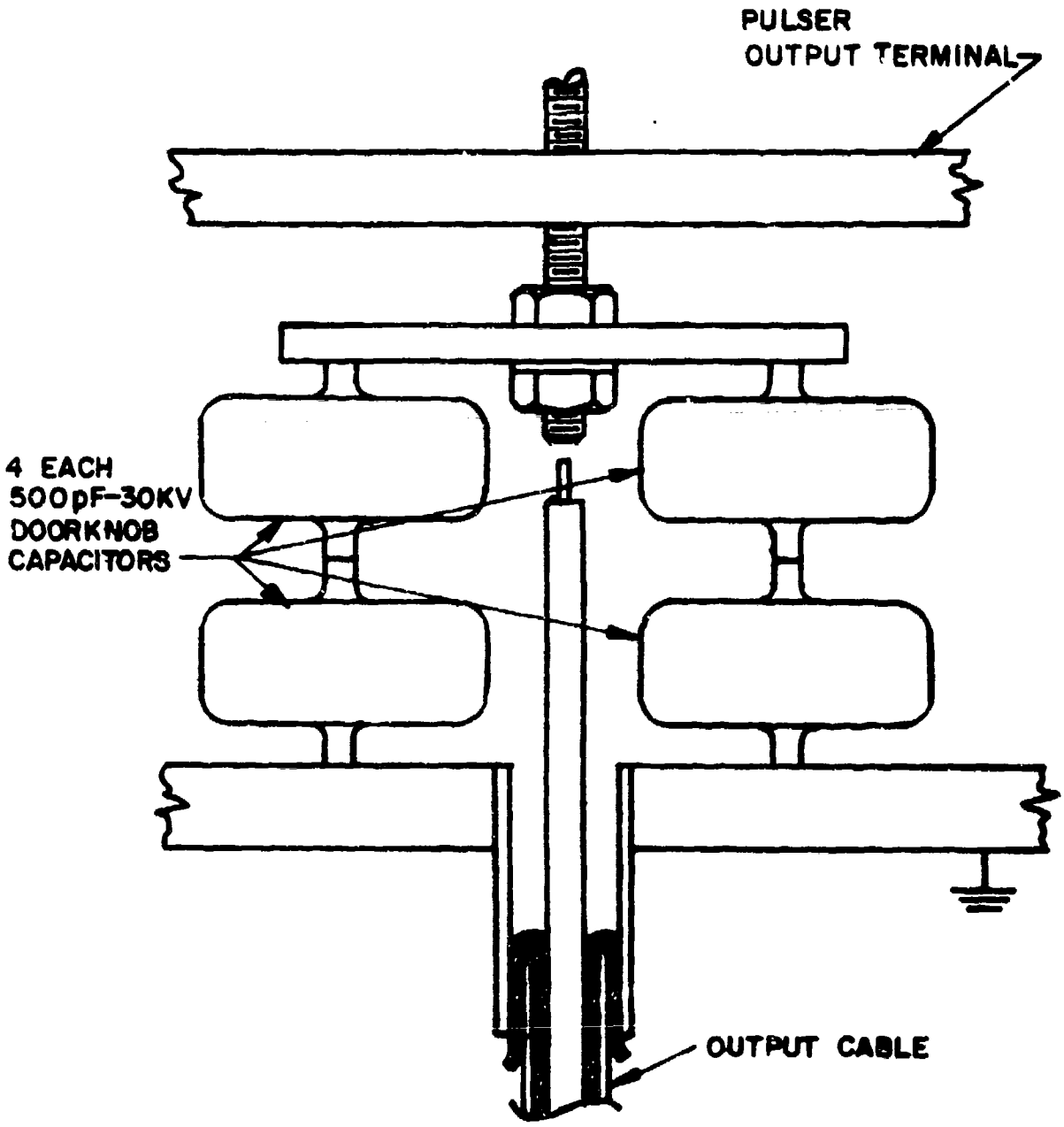


Figure 26. Third Gap with Doorknob Capacitors

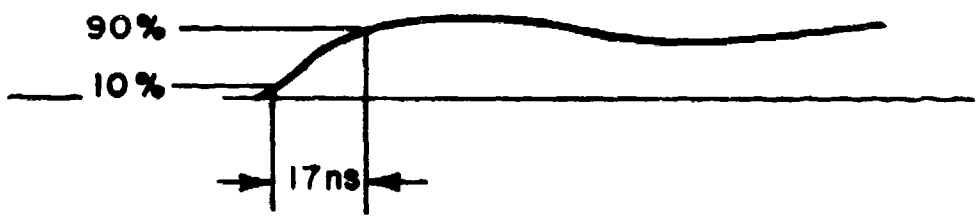


Figure 27. Output Current Pulse with Doorknob Capacitors

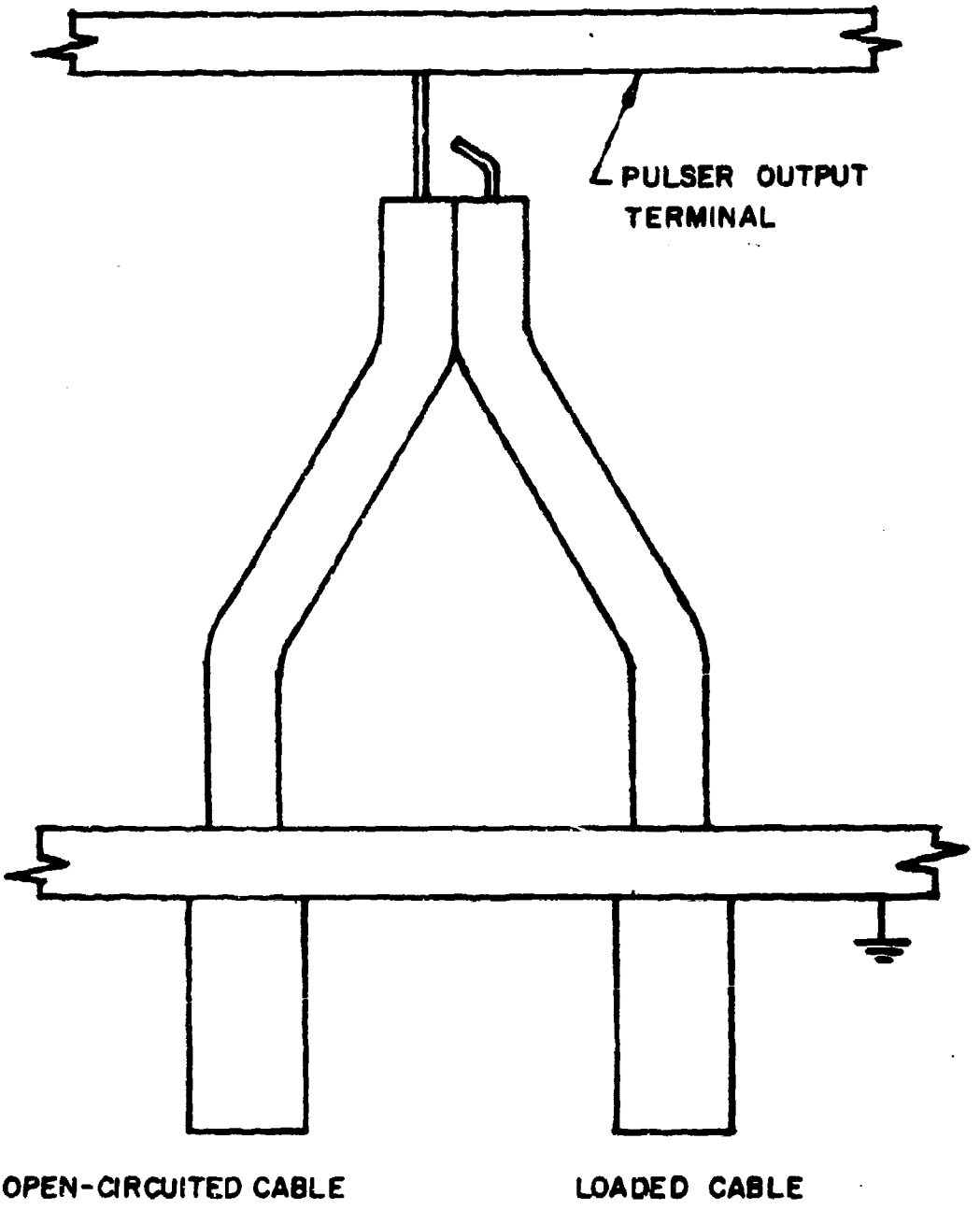


Figure 28. Third Gap with Open-Circuited Cable

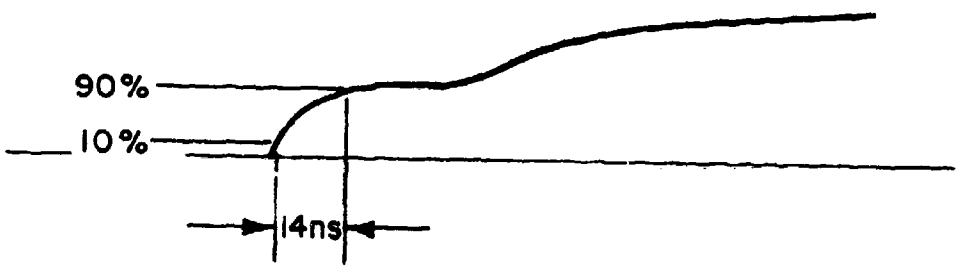


Figure 29. Output Pulse with Third Gap and Open-Circuited Cable

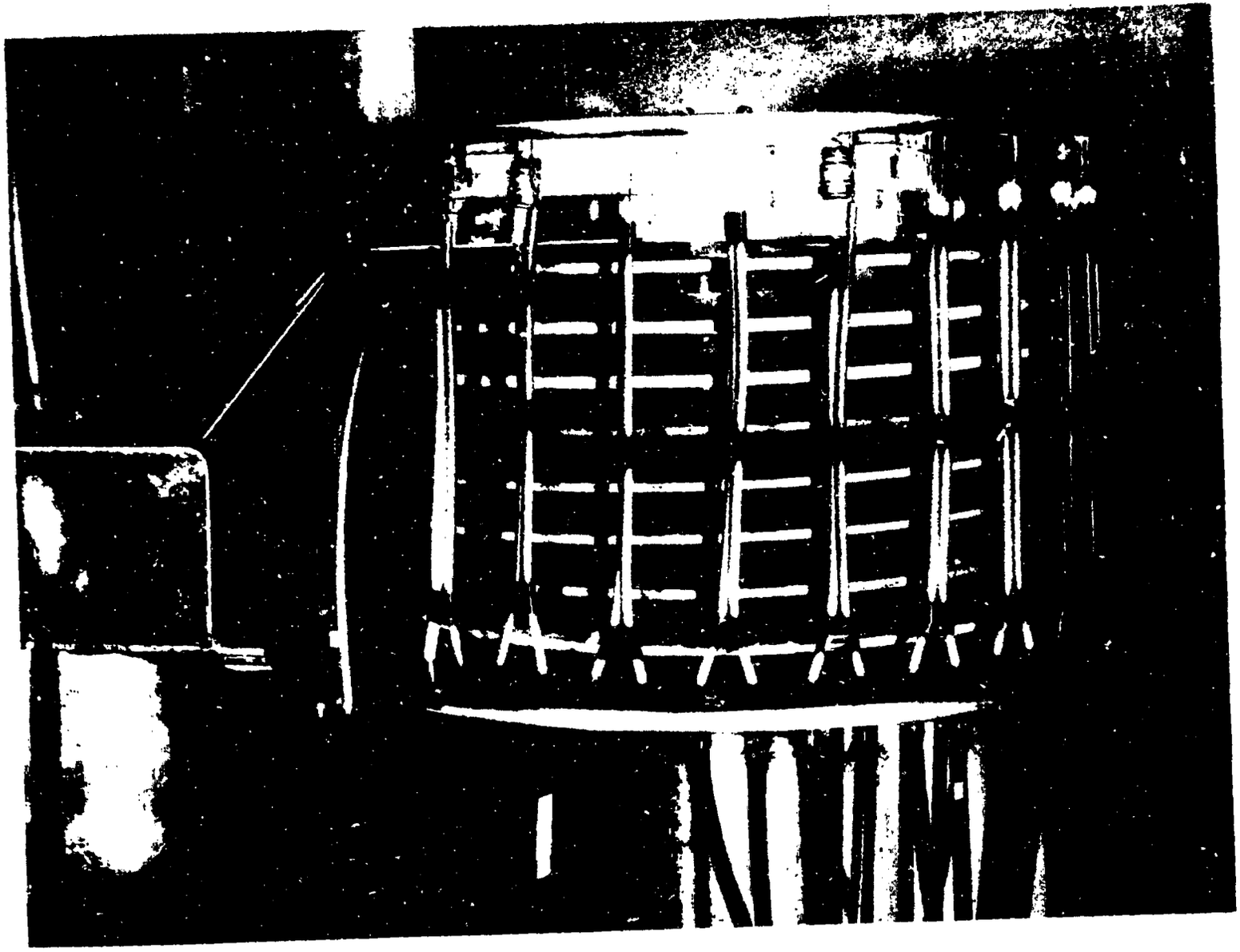


Figure 30. High Speed Pulser for EMP Simulator

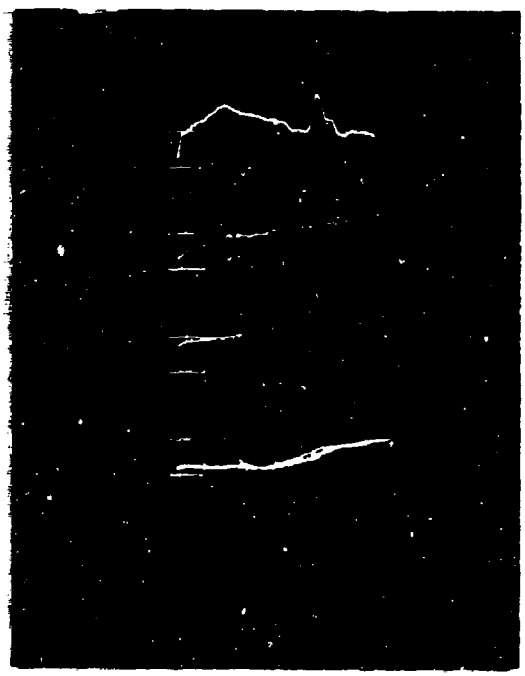


Figure 31. Jitter Measurement

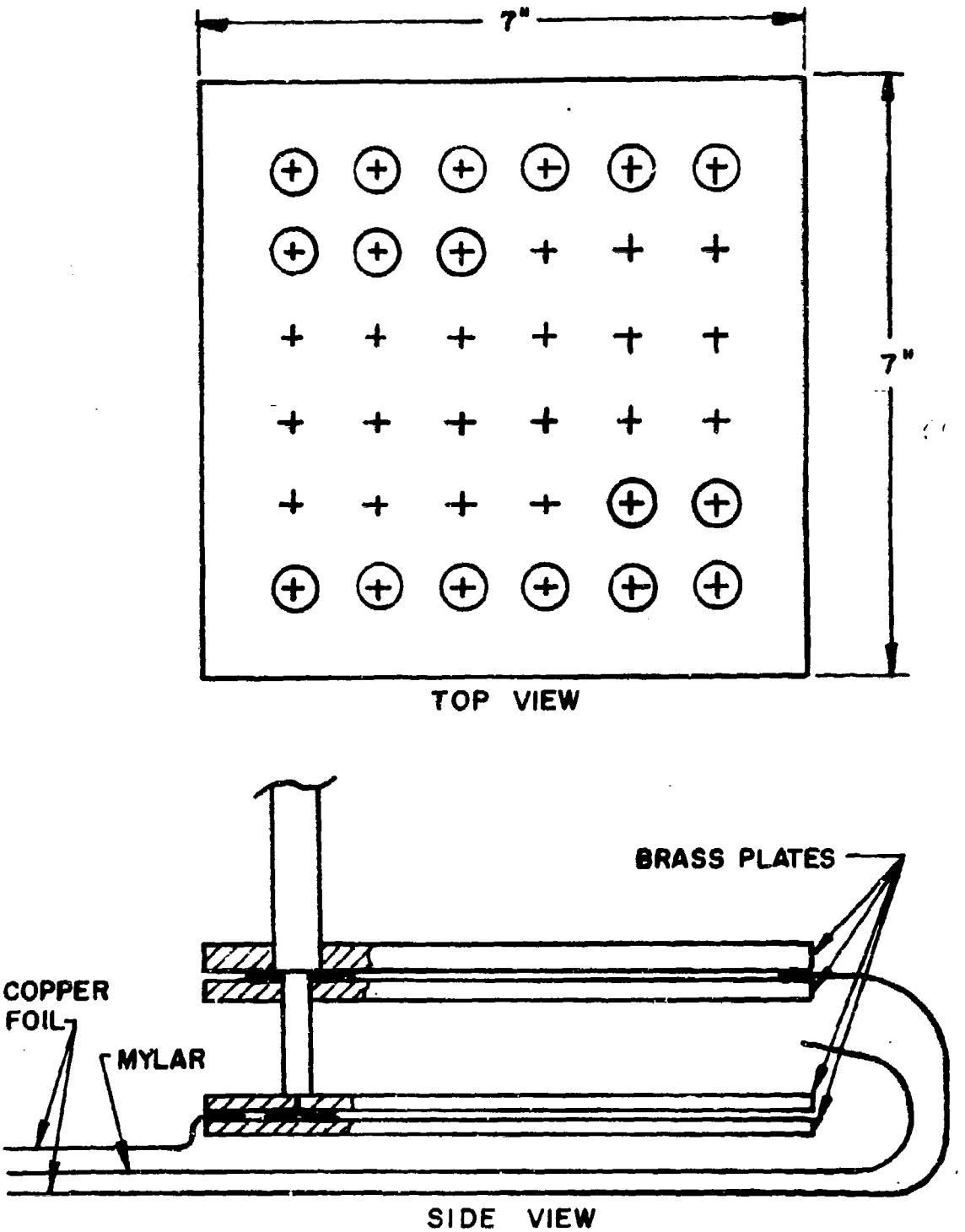
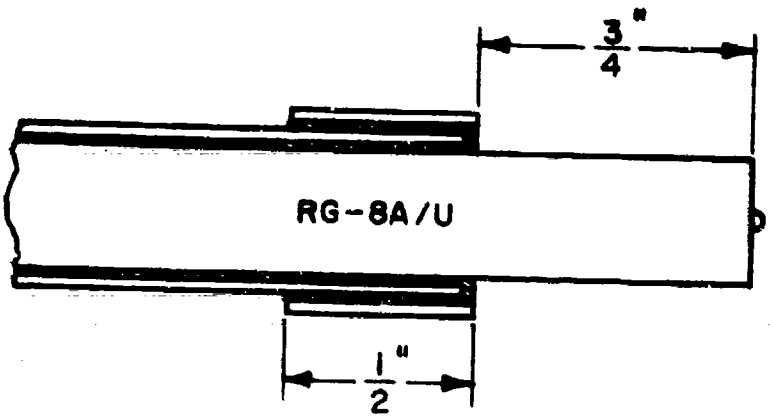
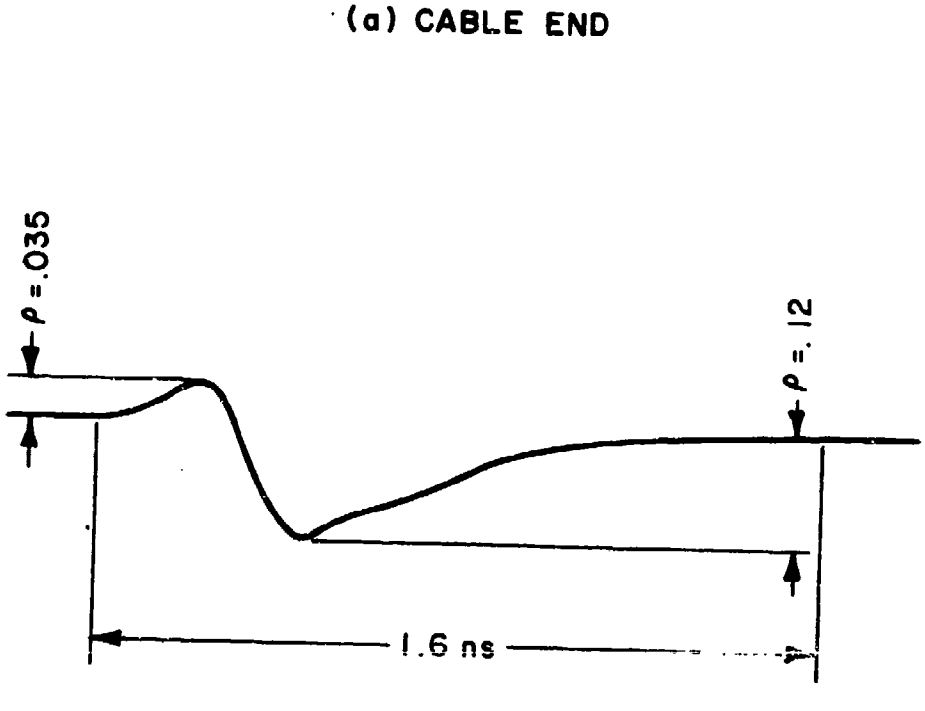


Figure A-1. Coax Load Resistor

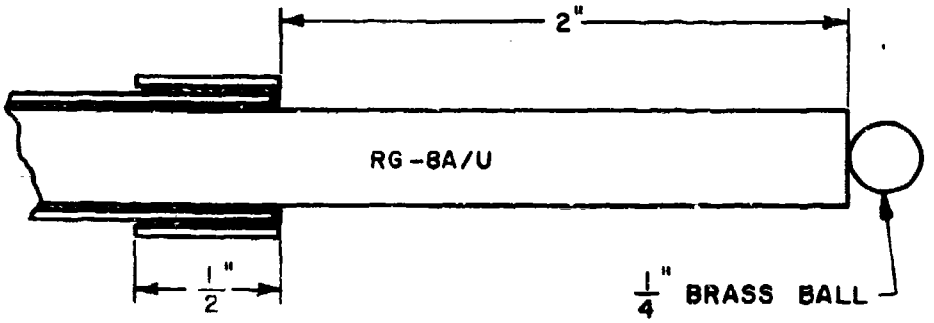


(a) CABLE END

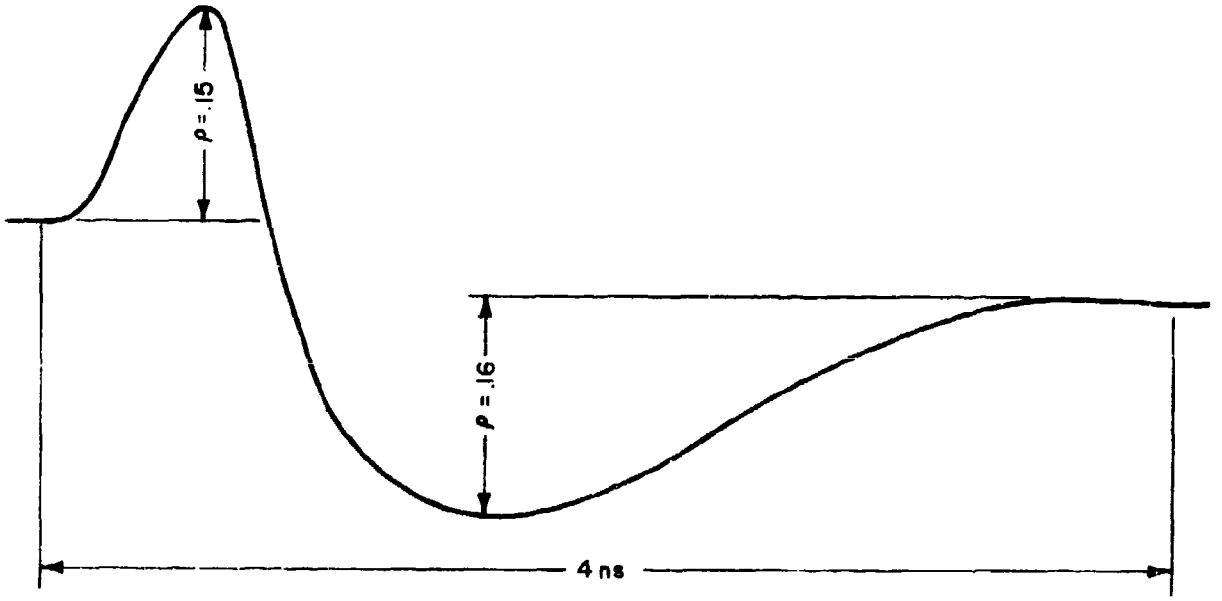


(b) TDR TRACE

Figure A-2. Cable End with Optimum Configuration



(a) CABLE END



(b) TDR TRACE

Figure A-3. Cable End with Reduced Current Density

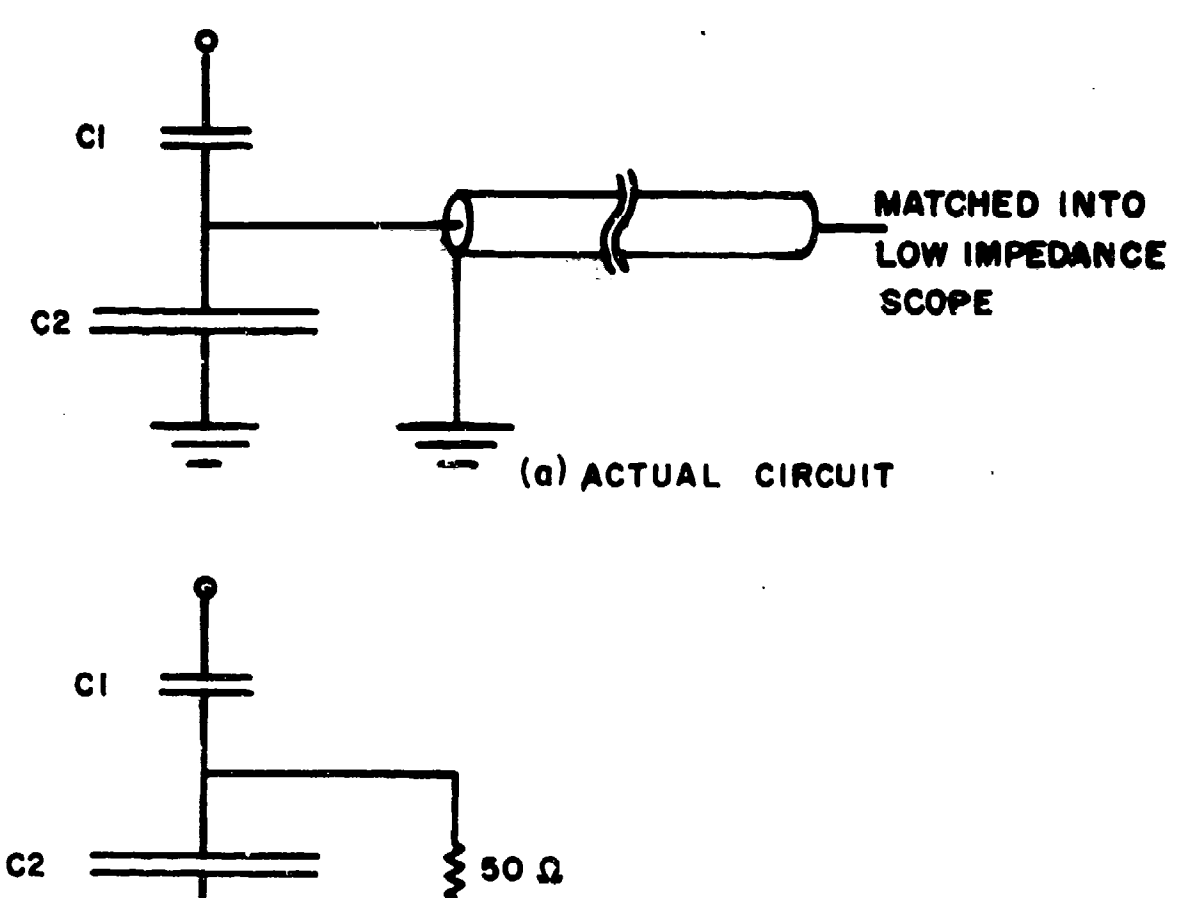


Figure B-1. Capacitive Divider Loaded with Cable And Scope

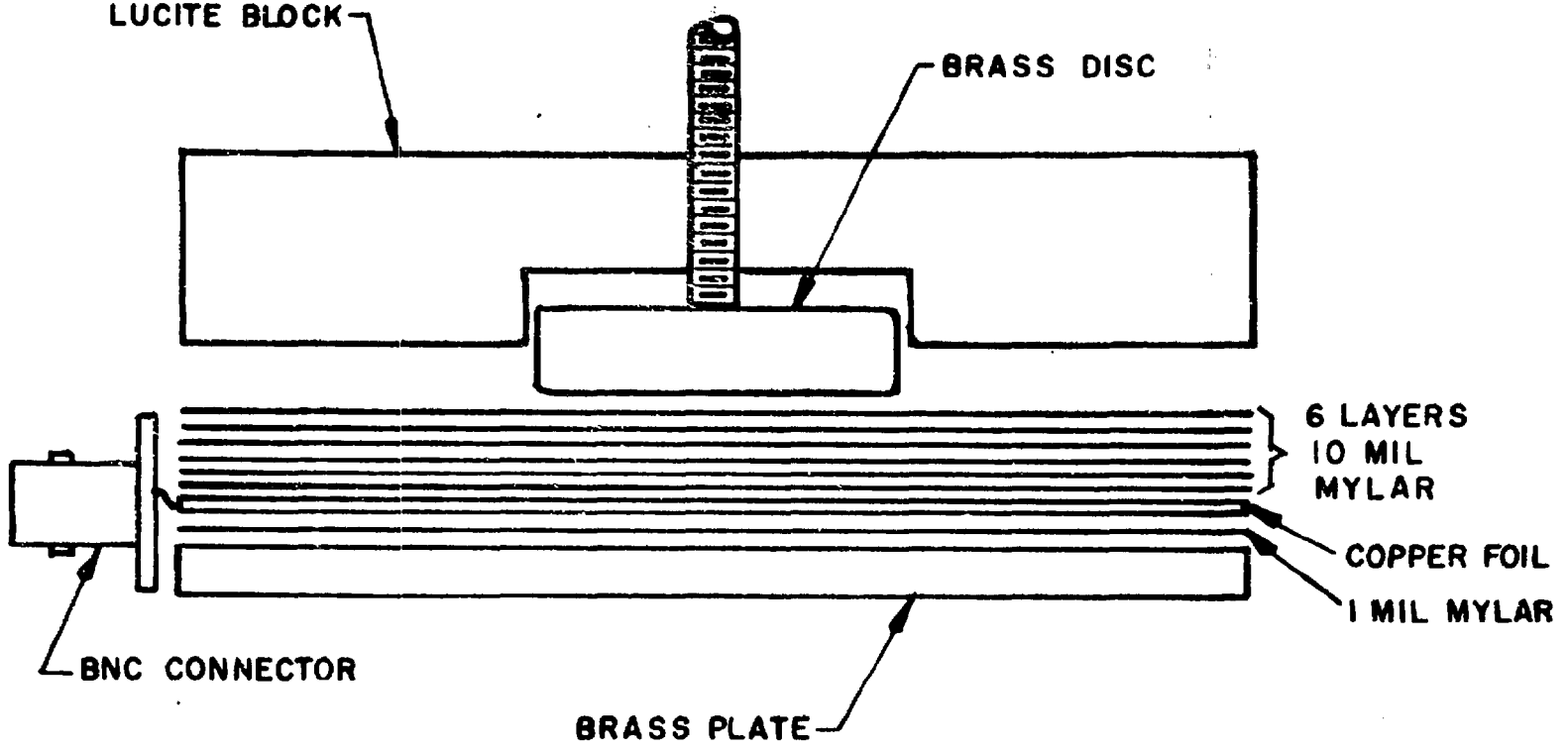


Figure B-2. Low Impedance Capacitive Divider

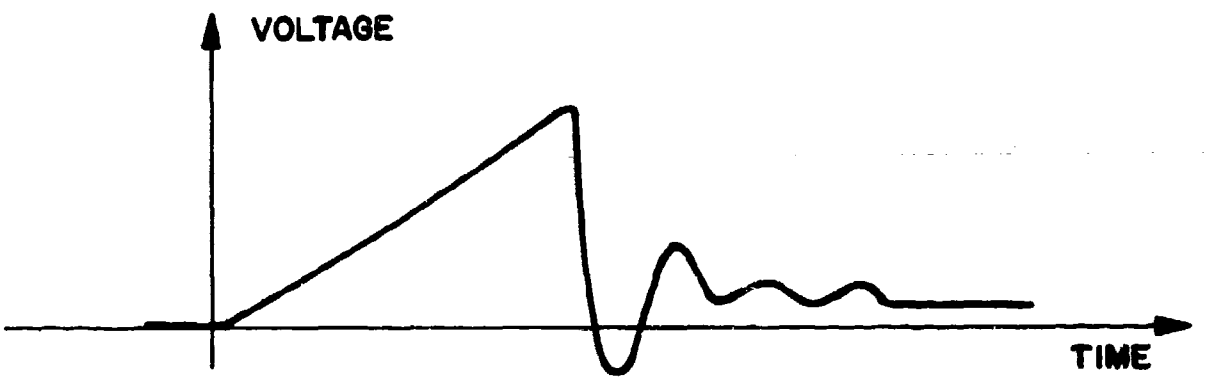


Figure B-3. Scope Protection During Flashover of Capacitive Divider

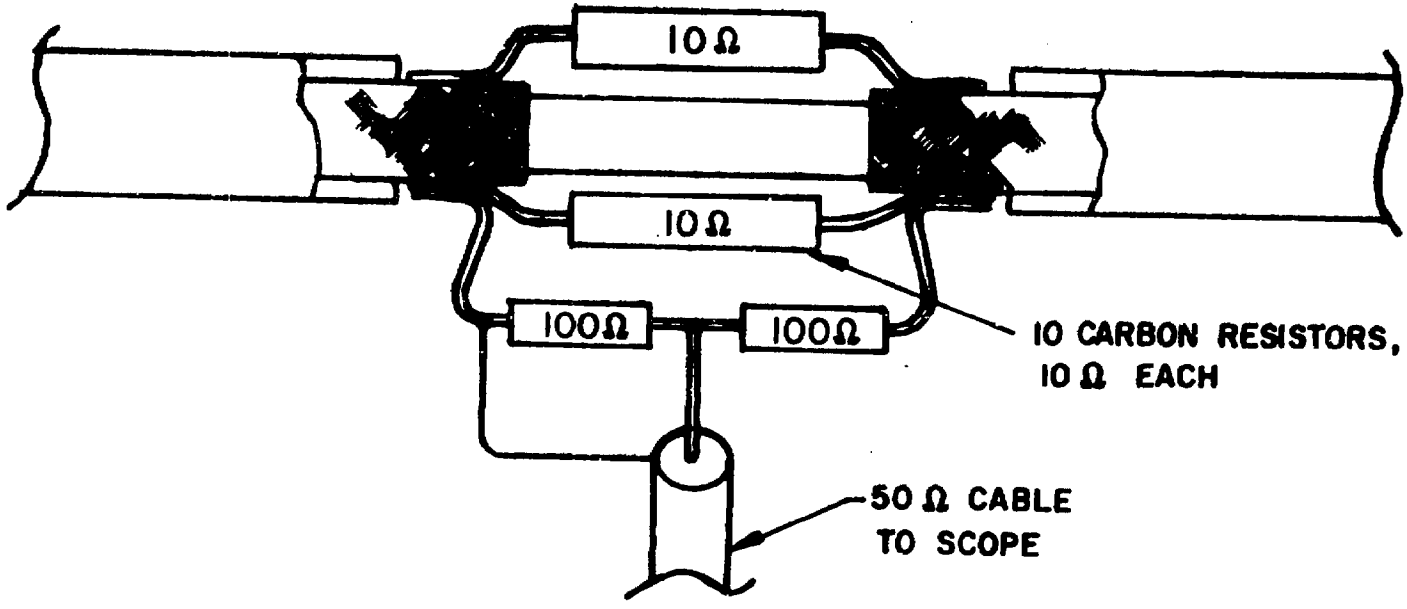


Figure B-4. Carbon Current-Viewing Resistor

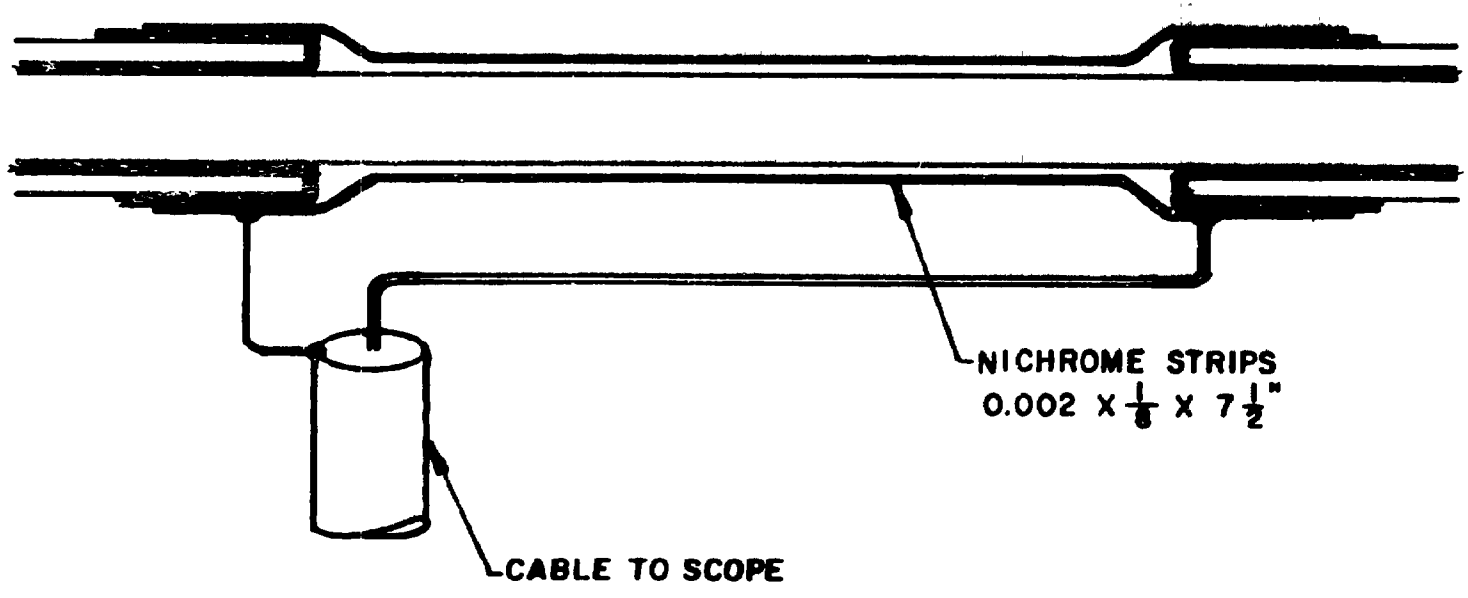


Figure B-5. Nichrome Strip Current-Viewing Resistor

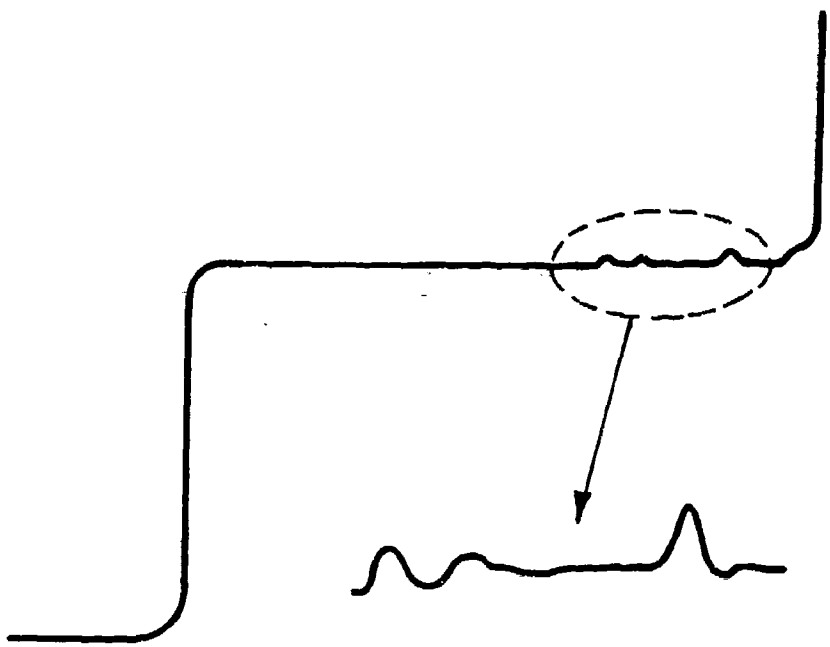


Figure B-6. Time Domain Reflectometer Trace of Nichrome Resistor

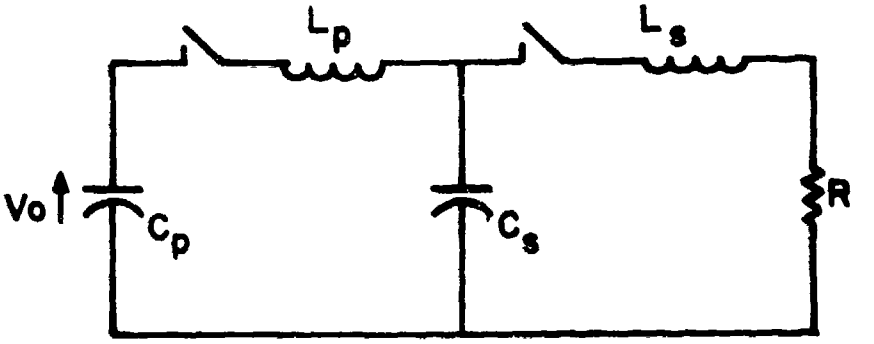


Figure C-1-a. Actual Two-Loop Circuit

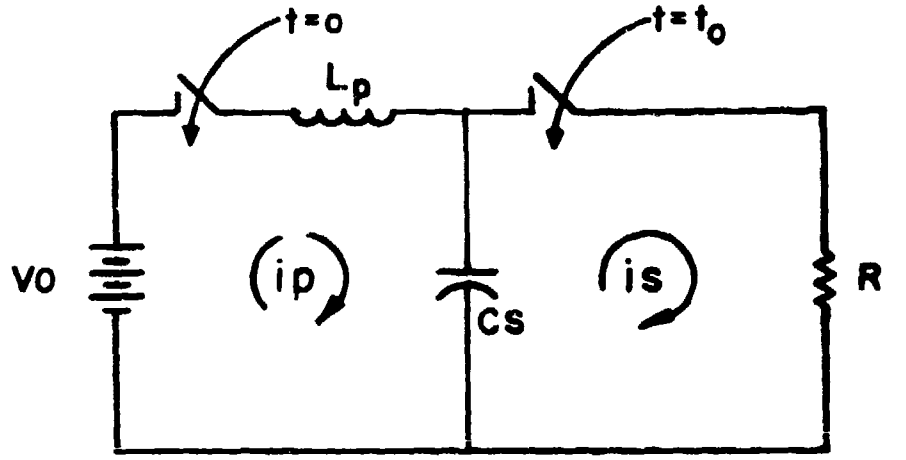


Figure C-1-b. Simplified Two-Loop Circuit

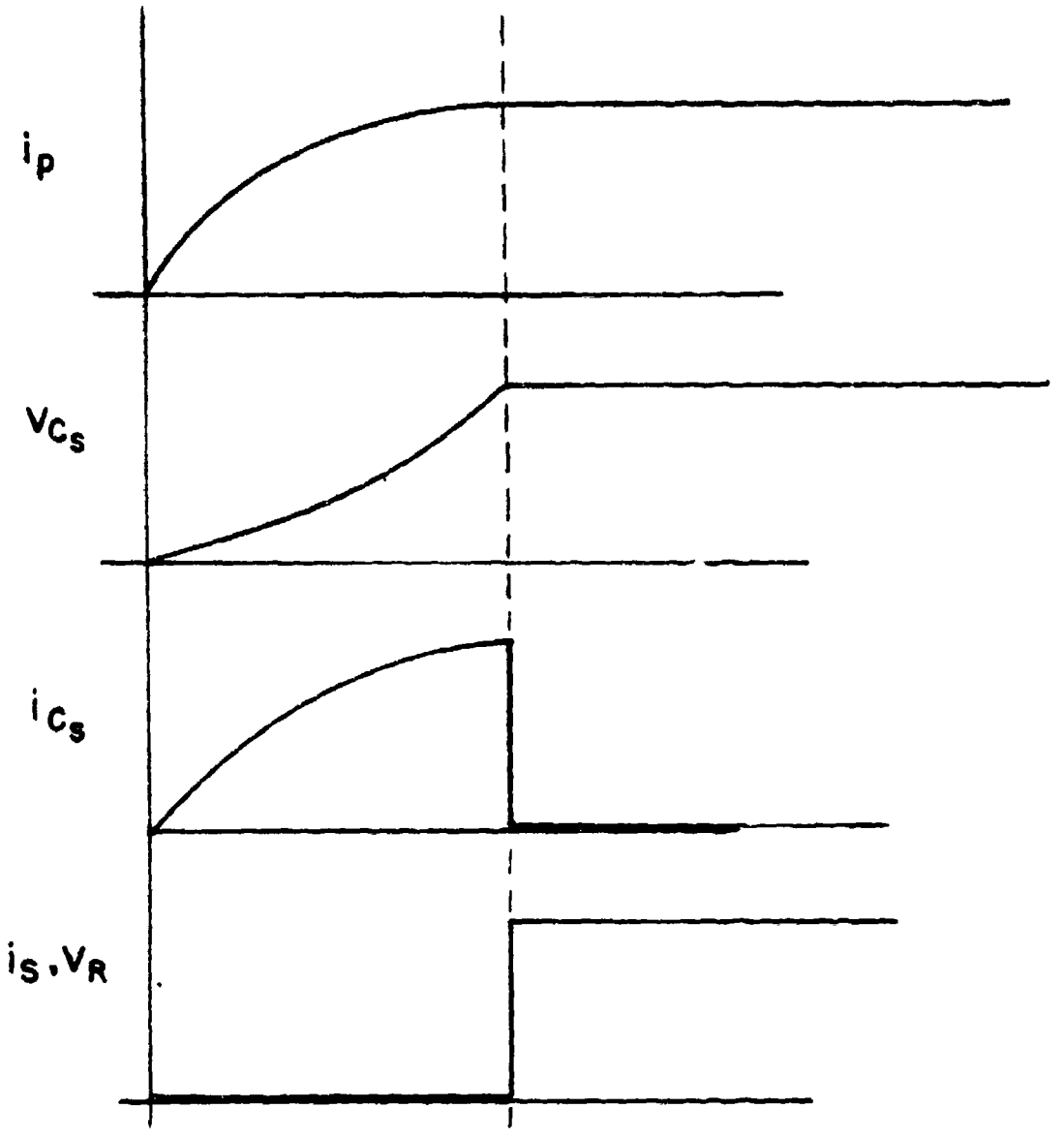


Figure C-2. Waveforms in Simplified Two-Loop Circuit

FIG. C-2

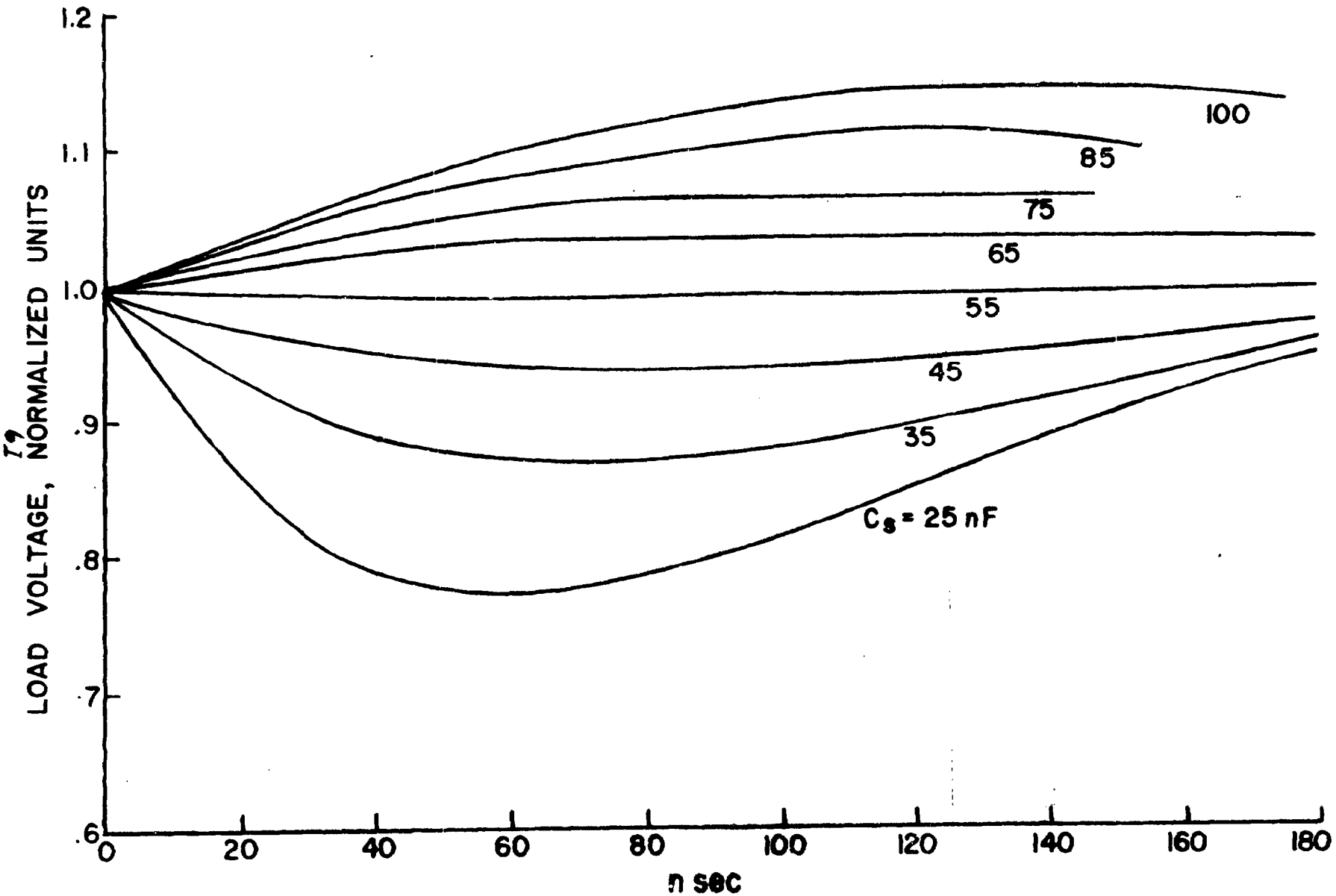


Figure C-5. Load Voltage Pulse Shape, C_S as Parameter

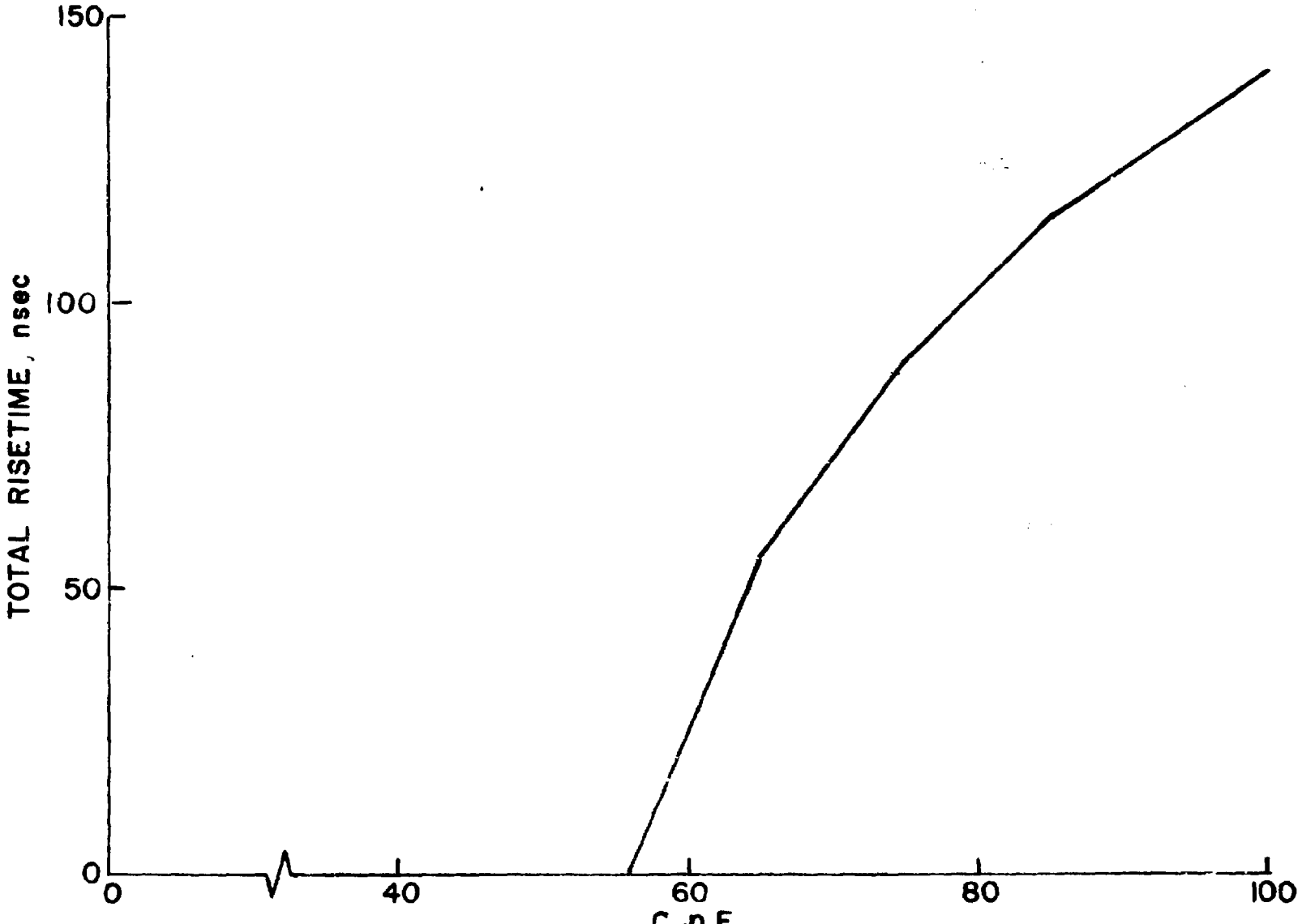


Figure C-4. Risetime Versus Peaking Capacitance

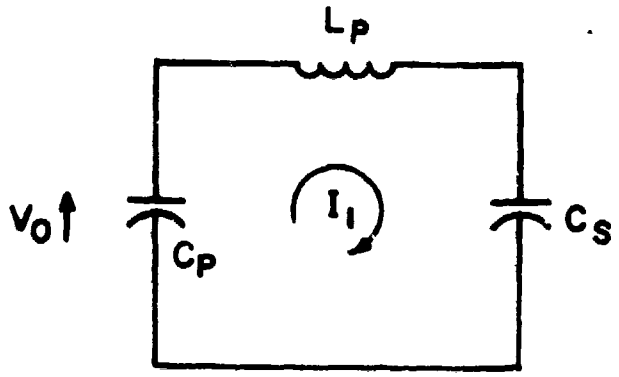


Figure C-5-a. Primary Loop Before Closing Sharpening Gap

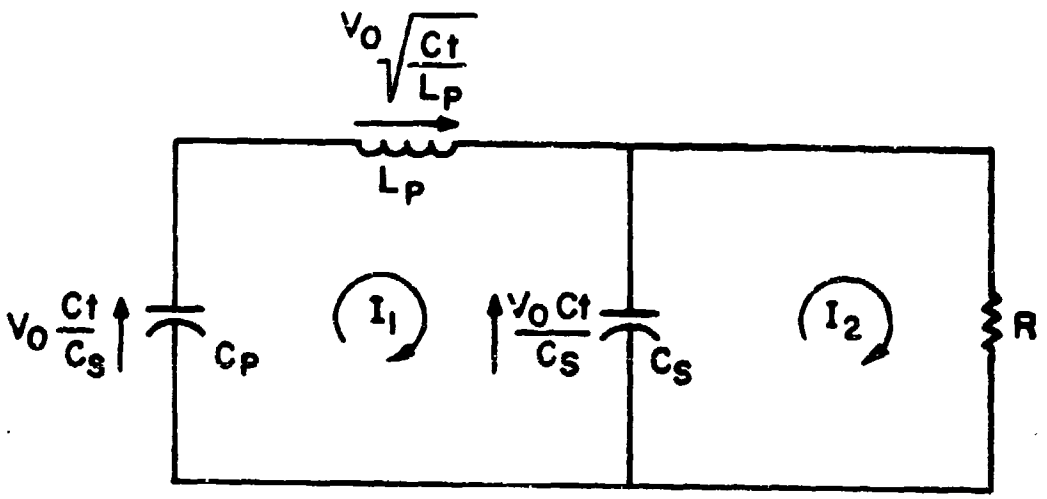


Figure C-5b. Circuit After Closing Sharpening Gap

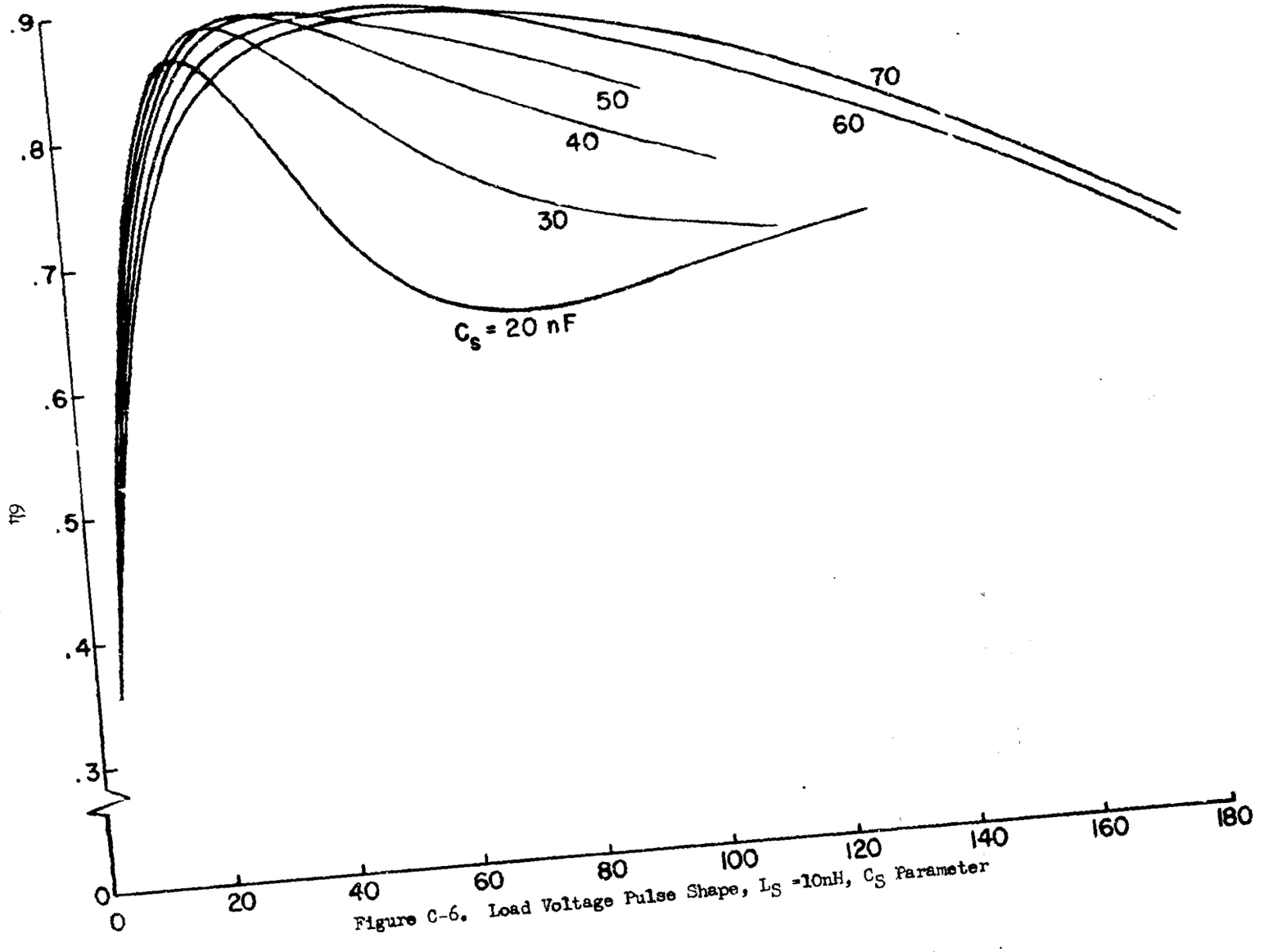


Figure C-6. Load Voltage Pulse Shape, L_S =10nH, C_S Parameter

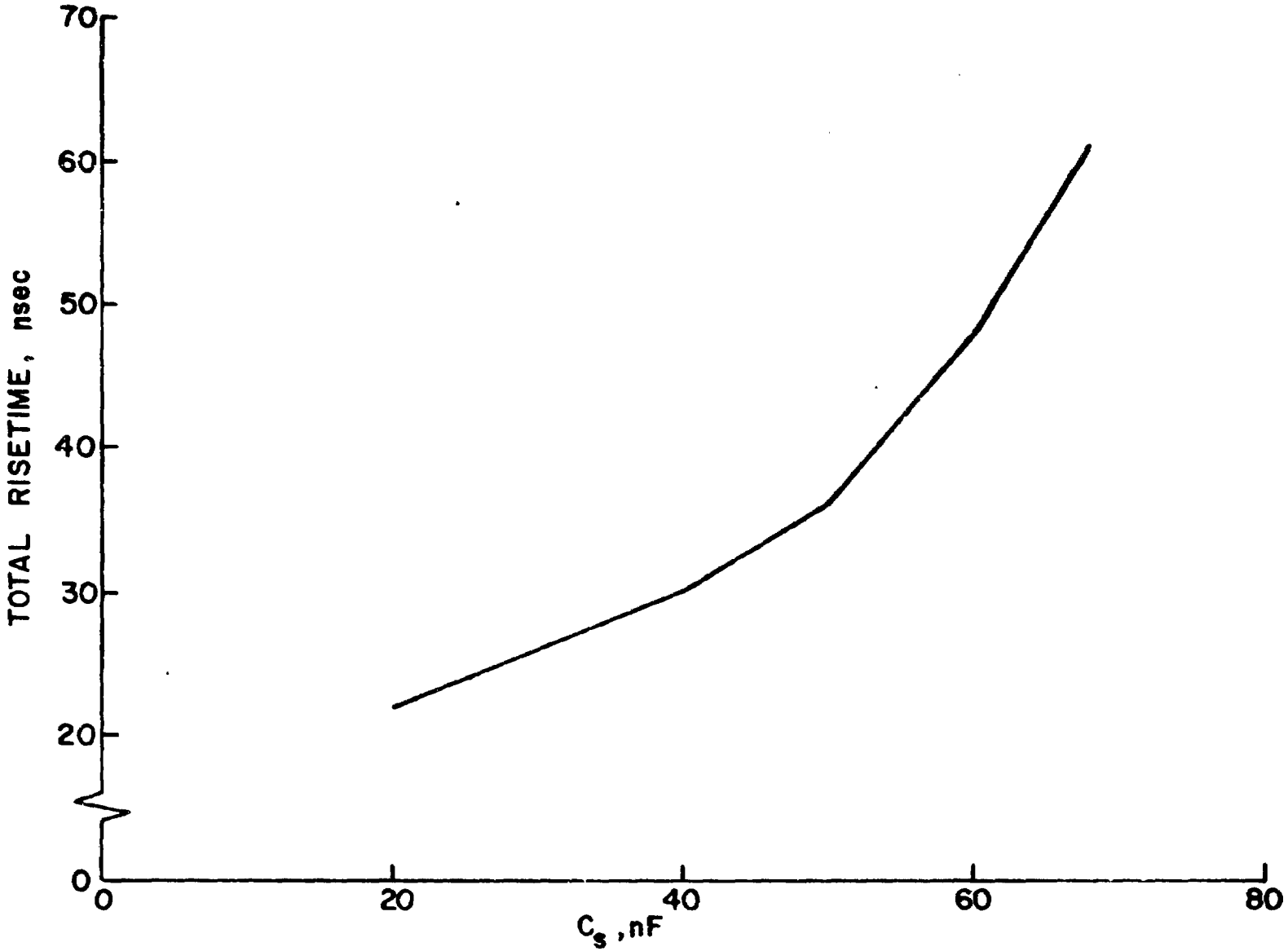


Figure C-7. Total Risetime Versus Peaking Capacitance, L_S =10nH

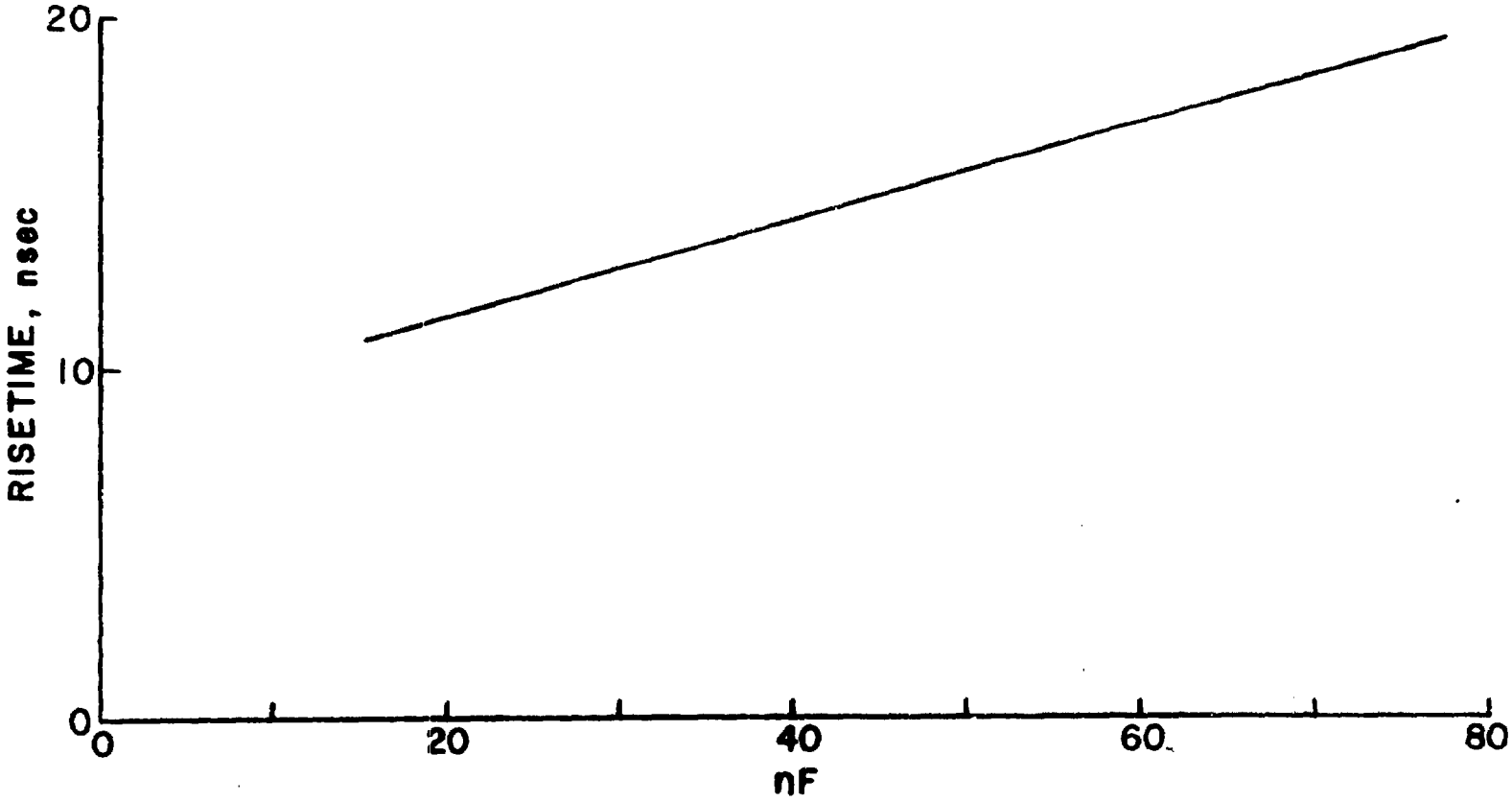


Figure C-8. 10%-90% Risetime Versus Peaking Capacitance, L_S =10nH